NOAA/SBIR
Contract # DG133R06CN0158

FINAL Report
for the
Design and Specification
of the
DCP Command Link

14 Jun 2009

© Sutron Corp
22400 Davis Drive #101
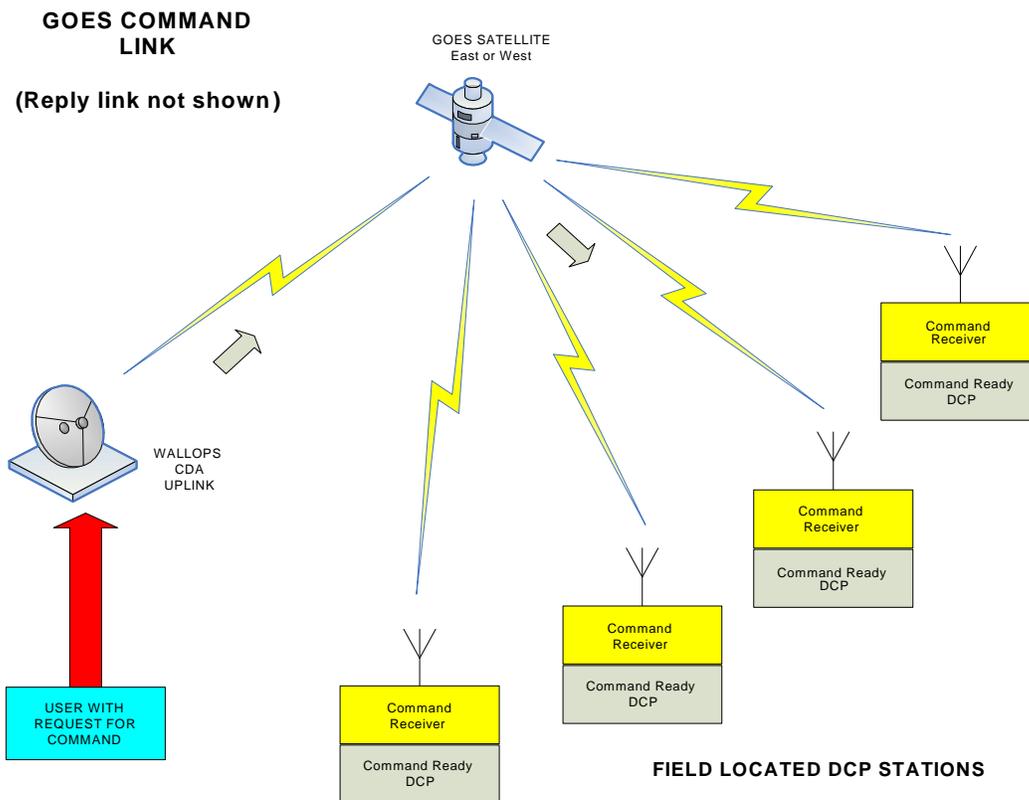# Sterling, VA 20164

703-406-2800

This material is based upon work supported by the Department of Commerce under contract DG133R06CN0158. Any opinions, findings, conclusions or recommendations expressed in this publication are those of the author(s) and do not necessarily reflect the views of the Department of Commerce.

Summary

This document is the final report of Sutron's work to provide a design and specification for a new Data Collection Platform Command (DCP) Link to replace the now defunct DCP Interrogate capability.   Sutron has built on the results of the phase one study and successfully built and tested prototypes. It is Sutron's belief that most all key objectives have been met and the system is a resounding success. Sutron is ready to assist the government to proceed to the next level of DCPCommand operation.

GOES COMMAND LINK

(Reply link not shown)

GOES SATELLITE
East or West

WALLOPS
CDA
UPLINK

Command
Receiver

Command Ready
DCP

Command
Receiver

Command Ready
DCP

Command
Receiver

Command Ready
DCP

Command
Receiver

Command Ready
DCP

USER WITH
REQUEST FOR
COMMAND

FIELD LOCATED DCP STATIONS

Table of Contents

SUTRON 21300 RIDGETOP CIRCLE   STERLING, VA 20166   WWW.SUTRON.COM
(703)406-2800   (703)406-2801 FAX   SALES@SUTRON.COM

Table of Figures

Table of tables

SBIR PROJECT SUMMARY

This list below defines the key objectives set forth in the underlined SBIR proposal. Sutron will show how each key objective has been met and under what conditions.

1. Overall Design for the system has been proposed that is designed to operate in the vicinity of strong interfering signals.

The proposed design of the system from the modulation to the filtering of the front end of the receiver has been done to assist in the rejection of the interfering signals. These items include:

- Modulation scheme selected is an extremely robust technique in the presence of interfering signals. Spread Spectrum waveforms will reject strong interfering signals due to the fact that the interfering signal actually becomes spread across the modulation bandwidth just as the transmitted signal is de-spread to recover its signal.

- Double filtering at the receiver front end. A helical filter capable of handling the extreme power of an adjacent transmitter at 402 MHz and a double set of Saw filters around the passband help the receiver withstand most local interference. Filtering comes at the price of slightly higher noise figure. The decision was to leave the filtering in place at this time until further field testing may confirm operation near interfering transmitters.

The screenshot of Spectrum Analyzer's screen in Figure 1 shows that the passband of the receiver is relatively clean with no significant overloading signals present. Note the two tall signals, one on the left and one on the right are artifacts of the receiver and are not an issue. This measurement was taken at Wallops Island, VA although similar results were obtained at other locations.
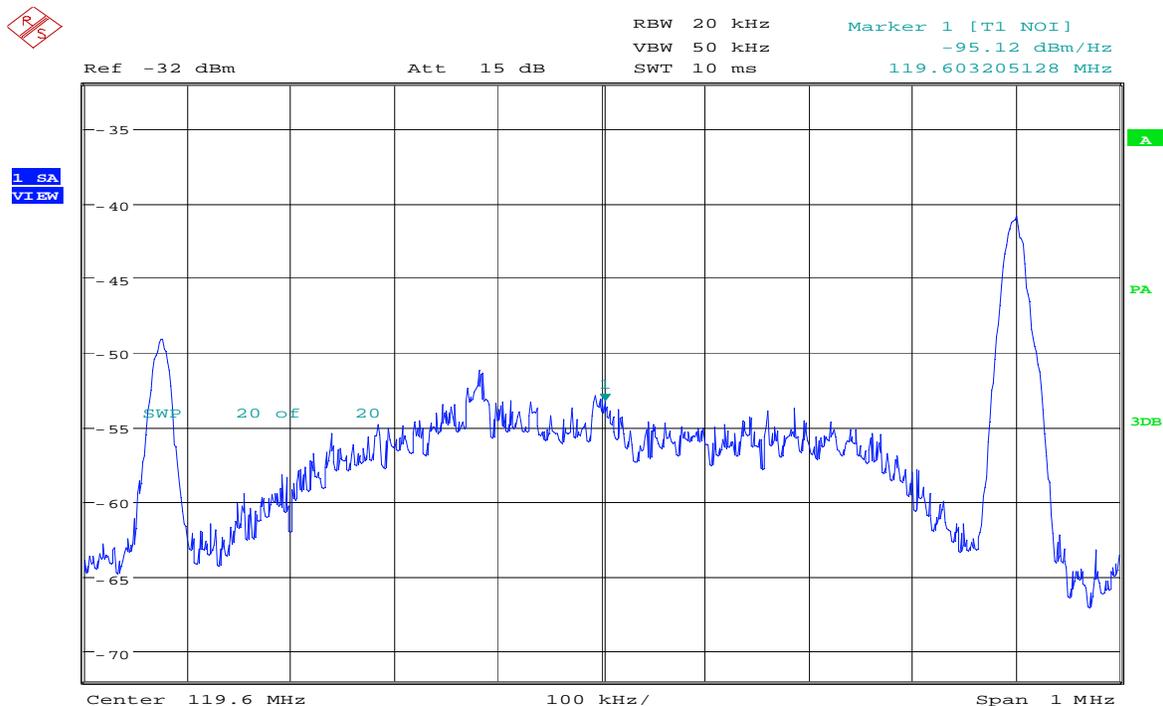
Figure 1: Spectrum of the passband of the DCPCommand receiver

- Future capability of adaptive filtering. The design approach will permit this at a later time.

2. Low cost hardware implementation approach.

The approach taken will yield a relatively low cost receiver. Very low cost components have been chosen for this project. The DSP portion of the system is the most expensive.

- A recommended hardware implementation approach with low cost production targets has been provided. This was one of the key goals which is to keep the cost down on the remote hardware. Actual hardware costs of approximately 382 were incurred for the receiver with another $100 estimated for the antenna build yielding a total of $482. The addition of RS-232 and power cables will likely bring the receiver to exactly the targeted $500 board cost.

3. The use of the Reed Solomon code will provide valuable coding gain for the system. The original estimate for the receiver performance was a Bit Error Rate (BER) of 10^{-7}.

- Sutron achieved a very good performance in the presence of noise. The Figure 2 is the performance curve of the DCPCommand receiver. Note that the performance curve is a PFL but not a BER. The implementation loss as measured here is less than 0.5 dB. This closely approaches the desired performance levels.
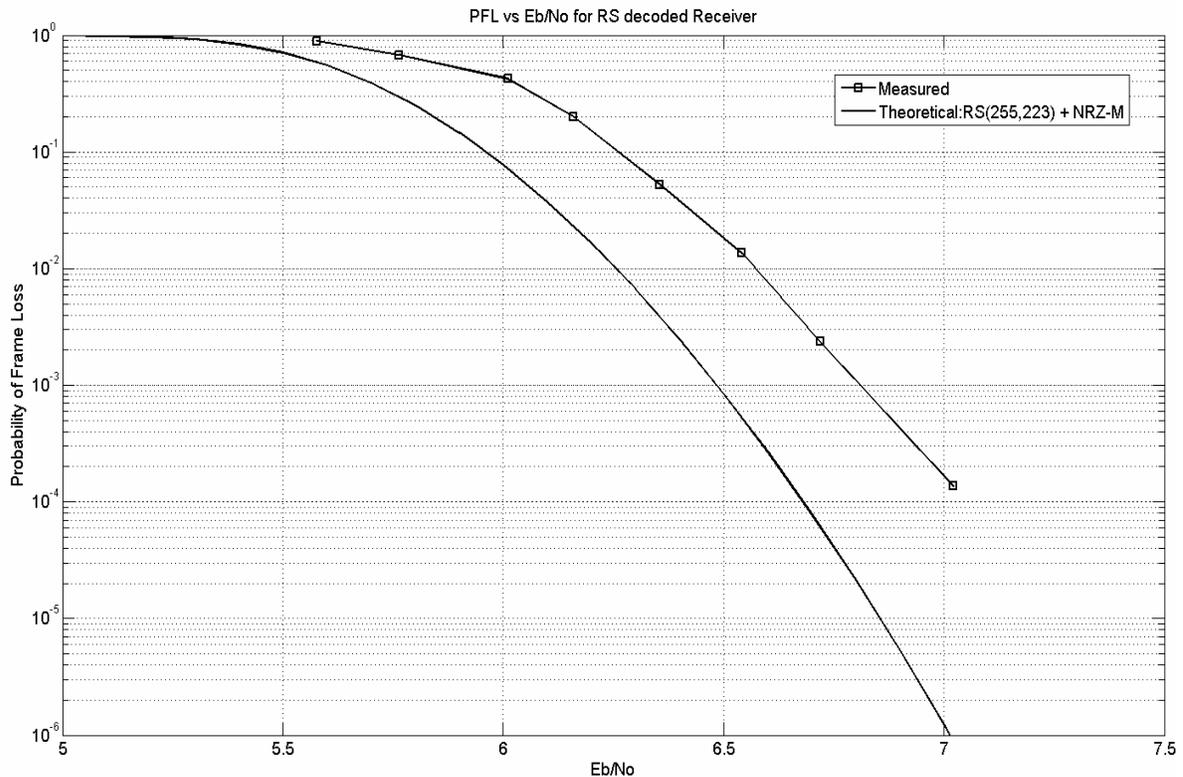
Figure 2: Probability of Frame Loss (PFL) versus Bit Energy-to-Noise ratio (E_b/N_o) of the DCPCommand receiver

4. Design a general protocol link. A data protocol has been presented that would provide a useful amount of data with a minimum wasted bandwidth.

- A protocol link has been designed to accomplish the task of logically transporting the data over the RF link established over the satellite. See Appendix A for the final recommendation. It is Sutron's belief that the link while a logical approach has been taken; some details of the link may be modified once the next level of implementation has been achieved at Wallops Island.

5. Designed tentative RF Communication Link. A CDMA technique has been proposed that will provide the ultimate possible protection from a Command Link from becoming jammed by a local strong signal.

- See the response to number 1 above. This goal has been accomplished.

6. Proposed solution meets the NTIA regulatory requirements resolving the issue of NESDIS loosing the frequency assignment for the DCPI/ DCP Command operation. Once that this is lost, it likely would be difficult for NESDIS to obtain it back.

- The original system failed the NTIA guidelines by almost 5 dB while the new system has a 3.5 dB margin with respect to the limits.

7. Designed to operate with simple low cost omni antennas. While it is not the intent of this SBIR to design the antennas, it is felt that relatively low cost antennas may be built or purchased to accommodate the receivers.

- Two antenna types were designed and built for this project in phase 2. The types chosen were done so due to their small size. The two antenna are:
  I. Quadrifilar Helix antenna. Figure 3 shows the antenna. This antenna has approximately 3 dB gain.
  II. Conical Helix antenna. Figure 4 shows the antenna. This antenna has approximately 6 to 7 dB gain.

Both antennas performed satisfactorily during the tests. Other antenna types are possible including micropatch antenna, yagi and possibly dipole type antenna.

Figure 3: Picture of Quadrafilar helix antenna

Figure 4: Picture of conical helix antenna

8. Designed to accommodate a high security and authentication system among users. This has been raised as a concern by various governmental agencies and this technique provided will assure that all DCPs will receive and process messages that are intended for them.

- This part of the system has not been implemented as it will be implemented at the Wallops Island uplink side first. Once that this is implemented, then implementation and testing on the receiver side will be done.

9. Designed to accommodate changes to the system easily via use of DSP based demodulation. This has proven to be a key concern as the system may undergo parameter changes. For example, if chip rate changes are made due to extended bandwidth availability, then that would likely only require a SW change

- Sutron did accomplish the complete demodulation process of the Direct Sequence CDMA modulation in software in a DSP. This will allow for software changes or upgrades with the simple download capability.

10. A significant advantage of the DSP system is the capability to add adaptive filtering techniques if nearby interference prove to be problematic. The DSP system can accommodate that change without any further hardware changes

- This system was not tested but may be added in the future if necessary.

11. Several design techniques to accomplish low power operation have been discussed. These are duty cycle operation of the receiver as well as cautious design of the hardware.

- These approaches have been considered and will be part of the system.

12. Performed general analysis to prove acceptable performance of the new link.

- Details to be provided later.

13. Ran models of the RF waveform for the DCPI Command signal confirming the expected RF waveforms.

- This was done and confirmed.

The following points were key issues during the **Phase 2** SBIR. Below is a recap of the issues.

Work Objective 1: Develop Demodulator Software on PC

The demodulator software will be developed and tested on a PC. This allows the development to proceed long before any real hardware is developed and available. Development on the PC is fast and benefits from the wide range of peripherals and tools that can be put to use. As the development of the demodulator software progresses, simulation data files will be generated containing a repeating data frame. These simulation files will be then be used to as test vectors for the de-spreading/demodulation algorithm.

Sutron can have a complete working demodulator running on the PC and perform a variety of tests on the operation and performance of the software. Among the test that will be run are test of signal acquisition, signal tracking and C/No performance.
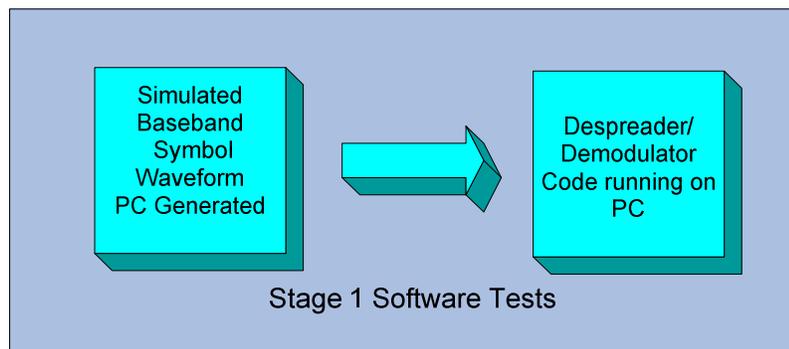
Figure 5: Simulation and testing on a PC

SUMMARY:

This was accomplished and served as a basis to continue on to the actual hardware/software implementation.

Work Objective 2: Develop New Receiver Board

2.1 Design

The overall system will consist of 2 Printed Circuit Boards (PCB): a receiver board and a processor board. Work Objective 2 develops the new receiver board. The phase I work created a block diagram of the new receiver and explored chips that could be used to implement critical receiver functions efficiently. Sutron will use that preliminary design to create a complete design (schematic) for the new receiver board. This new board will follow all usual design processes at Sutron and be designed for the correct levels of ESD and Surge protection.

2.2 PCB Layout

Once the receiver board design is complete, Sutron will proceed with the layout of the PCB. The first hardware prototype will be a multilayer designed RF board. Sutron has full control of the PCB design process including the placement of size and type of components, component placement, routing of traces, and shielding. Once the bare board is designed, Sutron will manufacture a small number of boards, assemble them and then test them to verify and validate proper operation. Usually a second iteration of the PCB is required to resolve issues with the board and finalize the design and layout.

2.3 Test

The new receiver board is tested using Test Modulator (Work Objective 3). The receiver board will output I/Q data that, in turn, is fed to the PC running the demodulator software. This allows complete testing of the receiver using code already developed in Work Objective 1.
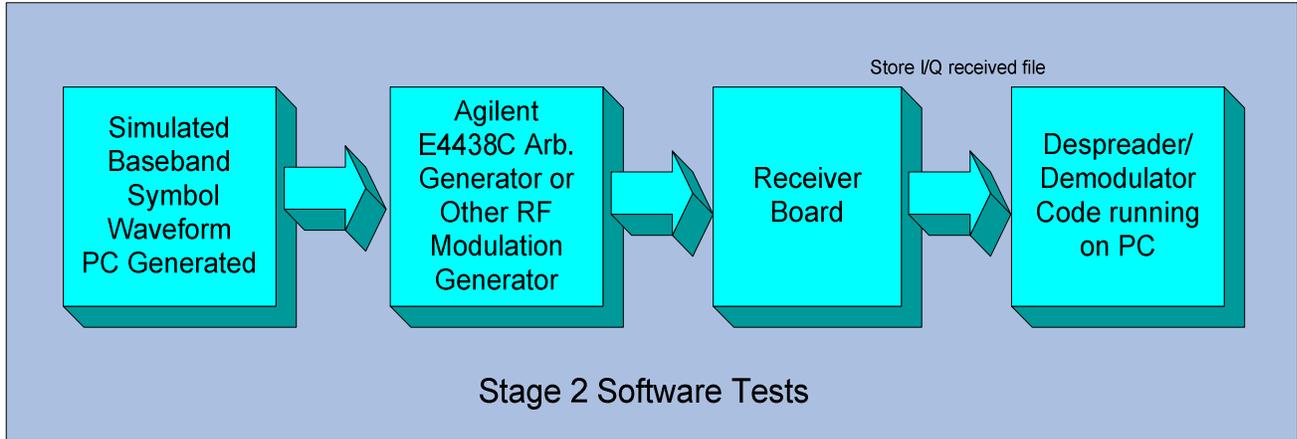
Figure 6: Testing the receiver board with the Test Modulator and Demodulator running on a PC

SUMMARY:

During the project, 2 prototype receivers were built. The first used an off the shelf DSP card with an off the shelf digitizer card coupled with the receiver board designed by Sutron.

The second prototype board was completely designed to reside on a single board. Below is an example of the final prototype. The microprocessor with display is a modified version of a standard Sutron product.
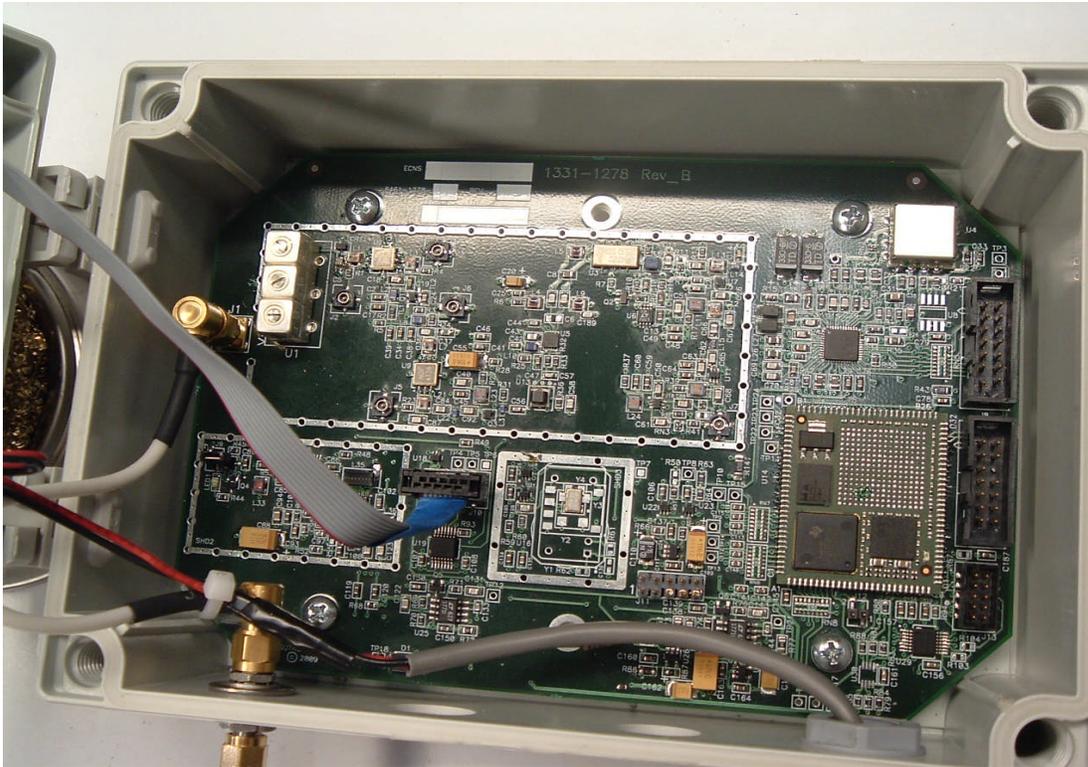
Work Objective 3: Develop Test Modulator

A test modulator will be developed for bench testing the receiver and for conducting tests at Wallops Island. The test modulator will be either be an 'off the shelf' piece of equipment or developed in-house, depending on which solution will achieve the desired test goal in the easiest and most usable fashion. An Agilent E4438C is a likely candidate for an off-the-shelf modulator, capable of generating baseband signals as well as RF test signals. With the '601' option of 8Msample memory the E4438C can generate at least 7 repeating frames of simulated DCP Command data (around 1.5minutes).

The test modulator will allow Sutron to:
- Transmit a fixed Frame Packet of data encoded with the spreading polynomial
- Ability to generate variable C/No levels
- Ability to modulate at different IF frequencies

SUMMARY:

This was accomplished early on with the use of an Agilent Signal generator. The generator has the capability to have the buffer loaded and it will repeat the message in a continuous fashion. The generator was used for development at Sutron and also was carried to Wallops Island for use to send signals over the satellite.

Work Objective 4: Port Code to DSP evaluation board for testing

Before starting the development of the final hardware, Sutron will port the demodulator code to a DSP board for further testing. The purpose of this is to begin the process of testing the software that has been developed on a PC and porting the code to run on the DSP processor. While this processor card is not the final target hardware, it will serve to point out any performance issues before the first board is designed.

The code running on the DSP board will allow Sutron to verify that the demodulator software runs on the limited hardware of the DSP. The performance of the DSP can be studied to ensure that there is adequate resources for the software and to verify the power consumption of the product. With these items confirmed, the development of the processor board (Work Objective 5) can proceed with a minimum of risk.

SUMMARY:

This objective has been accomplished and was demonstrated on the first prototype.

Work Objective 5: Develop Prototype DCPC receiver.

This work objective designs the final prototype DCP Command receiver. There are a number of steps to accomplish this objective:

5.1 Mechanical Design and Packaging

A detailed mechanical design will be done with the goal of achieving the near final packaging dimensions for all the circuit boards as well as the initial packaging design. The physical dimensions chosen here will determine the dimensions for the prototype receiver and controller/DSP card.

5.2 Design controller/DSP card.

This work proceeds with the schematic design, followed by the layout and manufacturing of the resulting board. As was the case for the receiver board, all aspects of the design are under Sutron's control. The design will be based on the evaluation board along with clock, interface and power circuits used by Sutron in other products.

5.3 Build controller/DSP card Prototype and checkout.

This will be the rudimentary testing that is required to bring new hardware to an operating level. Complete initial tests will include memory tests, A/D tests, I/O tests, and other RTC and detail functions. Testing of the quiescent current will be verified also.

5.4 Update and build receiver card layout

Modify Receiver and controller/DSP Artwork and Build Second Prototype. Following testing on the first prototype, changes and modifications will be edited into the board layouts. A new layout will be provided for both the receiver and controller/DSP card. Considerable focus will be spent reducing the size of the prototype.

5.5 Build Mechanical Packaging hardware.

5.6 Port code and run on new target receiver prototype

This level testing will involve the porting of the controller/DSP code previously tested on a PC to the target system. The received signals will now pass through the entire receive chain that is the first cut of hardware.
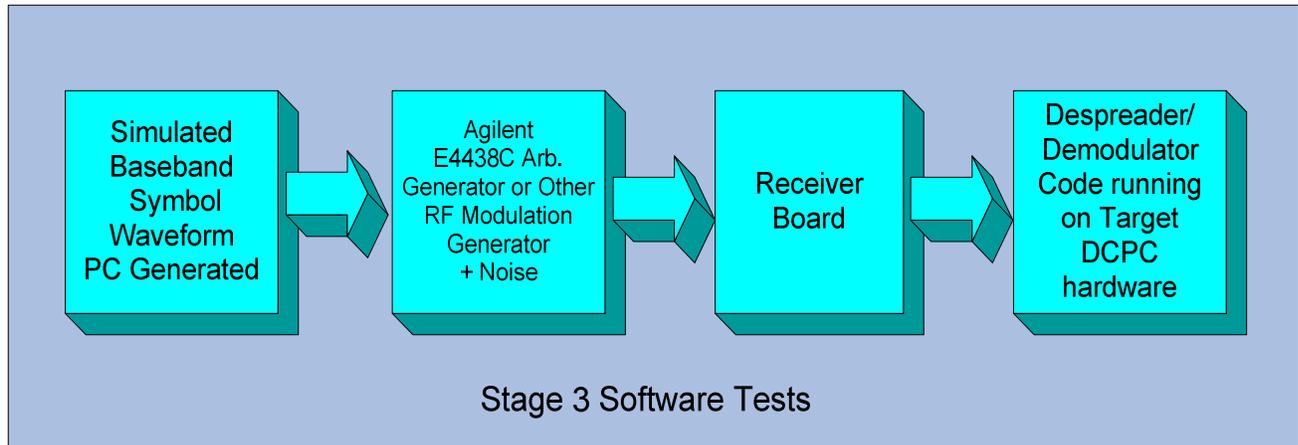
Figure 7: The block diagram shows concept of simulation and testing running on target hardware.

SUMMARY:

For sections 5.1 through 5.6, all goals are met again by virtue of demonstrating the prototype receiver.

5.7 Complete Bench Performance testing

The new hardware for both the receiver and controller/DSP card will be tested and integrated. All sections of the hardware will be tested and verified against the original design goals. Operational code will be downloaded into the hardware.

SUMMARY:

See section regarding the receiver testing.

5.8 Board revisions

After testing there is often a need to make revisions to the PCB in order to correct for defects in the initial design. Changes will be made to the PCB and additional boards will be manufactured to provide the final prototype units.

SUMMARY:

A second prototype was manufactured and shown in the pictures. This unit was taken to Wallops Island for testing.

5.9 Fabricate prototype units

The prototype units will then be fabricated. Sutron plans to make 10 prototype units of which will be used in Phase III tests. Sutron intends to retain all the prototypes; however, a certain number will be made available to NOAA for independent tests.

SUMMARY:

Sutron is in the process of manufacturing the units at the time of this writing.

Work Objective 6: Wallops Island Testing

6.1 Test System Integration for live receiver testing

Integrate Wallops Test system by modifying the test setup (WO3) to match the Wallops Island IF frequency and level. A key portion of this project will be the ability to test the receivers using live satellite signals. The satellite uplink signals are generated at Wallops Island Virginia at the NOAA NESDIS ground station facility. Sutron has the understanding at the time of writing this proposal that if a test signal conforming to the new DCPC format is modulated and mixed up to approximately 70 MHz, that the existing infrastructure may be able to properly uplink the signal to the satellite thereby allowing for a real 468MHz downlink signal from the satellite to the earth receivers. The test signal will be generated as mentioned in step 3 above and mixed appropriately to generate the proper IF signal.

6.2 Perform Wallops Tests

The setup that will generate the Wallops required signal will be taken to the Wallops Island station and setup for live tests. A test data packet will be used that will repeat in a continuous fashion as this is not an operational uplink system. The RF levels will be adjusted to fall within the expected C/No for downlink signal and the transponder AGC.

If this is not possible for any reason during this project's time case, the Agilent E4438C can easily provide a few mW of UHF simulated signal in to an omni antenna to simulate the satellite downlink for limited area outdoors testing.

SUMMARY:

A test was run at Wallops Island successfully. See the section below on testing.

Receiver Hardware Architecture Summary

The DCPC receiver consists of custom RF front end, an IF digitizing section, 16-bit fixed point DSP with 8Mbyte SDRAM and 512Kbyte Flash EPROM. A microcontroller with a display will be acting as an interface to monitor the activity and display the messages decoded by the DCPC receiver. The **Error! Reference source not found.** shows the block diagram of the DCPCommand receiver.
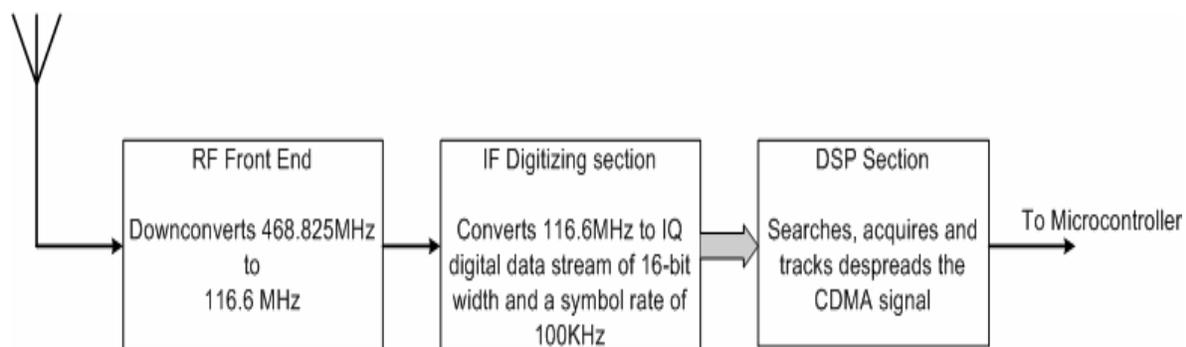
Figure 8: Block diagram depicting the DCPC receiver hardware architecture blocks

RF front end section

The custom RF front end along with an antenna acquires the RF signal centered at 468.825 MHz with a modulation 3dB bandwidth of 48 KHz. The RF front end applies the necessary noise filtering and gain control to down convert the RF signal to an IF signal centered at 116.6MHz. Helical filters are provided to assist in heavy front end overloading as may be seen with local 402 MHz transmissions from DCPs. Saw filters and the LNA help to define the overall operation of the system.

IF digitizing section

The down converted received signal was fed into an IF digitizing subsystem. This section converts the RF signal centered at 116.6MHz to a complex signal bandwidth of 100 KHz. The complex signal is digitized into 16-bit IQ data stream and fed into DSP via Serial Synchronous Interface (SSI). The IF digitizing subsystem utilized for this purpose was an Analog Devices AD9864.

The AD9864 consists of a low noise amplifier (LNA), a mixer, a band-pass Σ-Δ analog-to-digital converter (ADC) and a decimation filter with programmable decimation factor. An automatic gain control (AGC) circuit gives the AD9864 12dB of continuous gain adjustment. Auxiliary blocks include both clock and LO synthesizers. A Serial Peripheral Interface (SPI) allows configuring the parameters on the AD9864 such as synthesizer divide ratios, AGC attenuation and attack/decay time, received signal strength, decimation factor, output data format, 16dB attenuator and the selected bias currents .

An LO signal of 119.6MHz was provided to the AD9864 using an onboard VCO and the phase locked loop was set to track it using the SPI programming. Appropriate configuration was loaded into AD9864 to output a digital data stream at 16 bits per I and Q channel at a bit rate of 6MHz and a symbol rate of 100 KHz.

DSP section

The 16-bit IQ stream coming from the IF digitizing section will be processed by a 16-bit fixed point DSP processor. Texas Instruments TMS320VC5509A DSP was used for this purpose. The DSP buffers the incoming the IQ stream, searches and despreads the spread spectrum signal, and demodulates the resultant OQPSK signal. The demodulated signal goes through NRZ-M decoding and Reed-Solomon decoding resulting in the decoded messages. The decoded messaged are passed onto a microcontroller either for further processing or display.

The TMS320VC5509A DSP features a low-power fixed-point DSP core which can be operated at 108MHz or 144MHz or 200MHz, a 128K x 16-bit on-chip RAM, 64K bytes of on-chip ROM, six DMA channels, three Multipurpose buffered serial ports, two 20-bit timers, a JTAG emulation interface and other on-board peripherals. An external 8Mbytes of flash was used as external memory for store the firmware, used during the boot-up process of the DSP.

Receiver Software

The DCP Command receiver's software allows decoding the received signals with reconfigurable parameters. The entire despreading, demodulation and tracking of the baseband signal was done in software. The incoming IQ data stream was provided to the software as the input data and end result will be decoded messages and diagnostic information. The receiver software was written mostly in C programming language. Assembly language and libraries provided by Texas Instruments Code Composer Studio (TI CCS) were used in sections where execution speed and memory optimization was a priority. The TI CCS provided the required development environment to develop the receiver software. Spectrum Digital's XDS510USB JTAG emulator was used to communicate with the TMS320VC5509A DSP.

The receiver software can be broadly classified into (a) peripheral configuration and receiver management and (b) demodulator software. The peripheral configuration software involves configuring the peripherals, both inside and outside the DSP, to allow IF digitizing section configuration and, data transfers from IF digitizing section to the DSP and from DSP to a microcontroller. The IF digitizing section AD9864 needs to be configured during the

receiver start-up to facilitate the availability of IQ data stream to the demodulator. The receiver management software involves proper allocation of memory segments and buffer pools both statically and dynamically, setting up of Interrupt Service Routine (ISR) to allow real-time processing of the IQ data, managing the low-power schemes, and other housekeeping operations. Texas Instruments DSP/BIOS kernel was used extensively for receiver management software.

The demodulator software is a collection of software functions performing various tasks of receiver operation. The receiver operation can be represented as a state machine as in Figure 9.

The receiver enters into coarse search mode as soon as it receives a block of IQ data. The receiver will search for a carrier signal within the data by despreading the received spread spectrum signal with various coarse chip offsets of the PN sequence used to spread the transmitted signal. When the receiver convinces itself that there is presence of carrier signal for a given PN chip offset, receiver will enter the fine search mode. If the receiver feels that the carrier is not present, it will enter a wait mode for the next available block of IQ data.

The receiver in fine search mode will perform a fine search for frequency and phase of both carrier and PN sequence based on the estimates provided by the coarse search mode. If the fine search estimates are valid, the receiver will enter demodulation and tracking stage. Otherwise, the receiver will wait for the next IQ data block for coarse search mode.

The receiver in demodulation and tracking mode will be tracking the frequency and phase of both carrier and PN sequence using software implemented Phase Locked Loops (PLL). If the tracking of the parameters are valid, the receiver will continue to demodulate the incoming IQ data blocks. If the tracking of the parameters fails, the receiver will enter the Wait mode.

When the demodulation of an IQ data block is complete and the receiver has accumulated 4112 bits of NRZ-M decoded data, a search for frame sync marker will be made. If the search finds the sync marker, the receiver will perform the Reed-Solomon RS(255,223) decoding on the data for the messages. The RS decoding should correct up to 16 symbol errors in the decoded messages. The decoded messages are provided to a microcontroller over a SPI port on the DSP, for further processing. At present, the receiver provides diagnostic information along with the decoded messages such as number of corrections made by the Reed-Solomon decoder, whether the decoded message is error free or not, receiver calculated of bit energy-to-noise power ratio ($\frac{E_b}{N_0}$), elapsed time from last successful message decoding, carrier frequency offset and receiver state at the time of decoded message transmission.

In order to maintain the real-time operation of the receiver in processing the incoming IQ data stream, multiple buffering with Direct Memory Access (DMA) has been implemented. The multiple buffering scheme has provided the receiver to sustain a short break in reception of the signals and provides plenty of time to work on time-consuming tasks.

Receiver Diagnostics

These items below are potential diagnostics that could be obtained from the receiver, as of now. Many other metrics are potentially available.

- Bit energy-to-noise power ratio, Eb/No
- RS corrections/failures
- Decoded message is error-free or not
- Carrier frequency offset
- Elapsed time from last successful message decode
- Receiver state at the time of decoded message
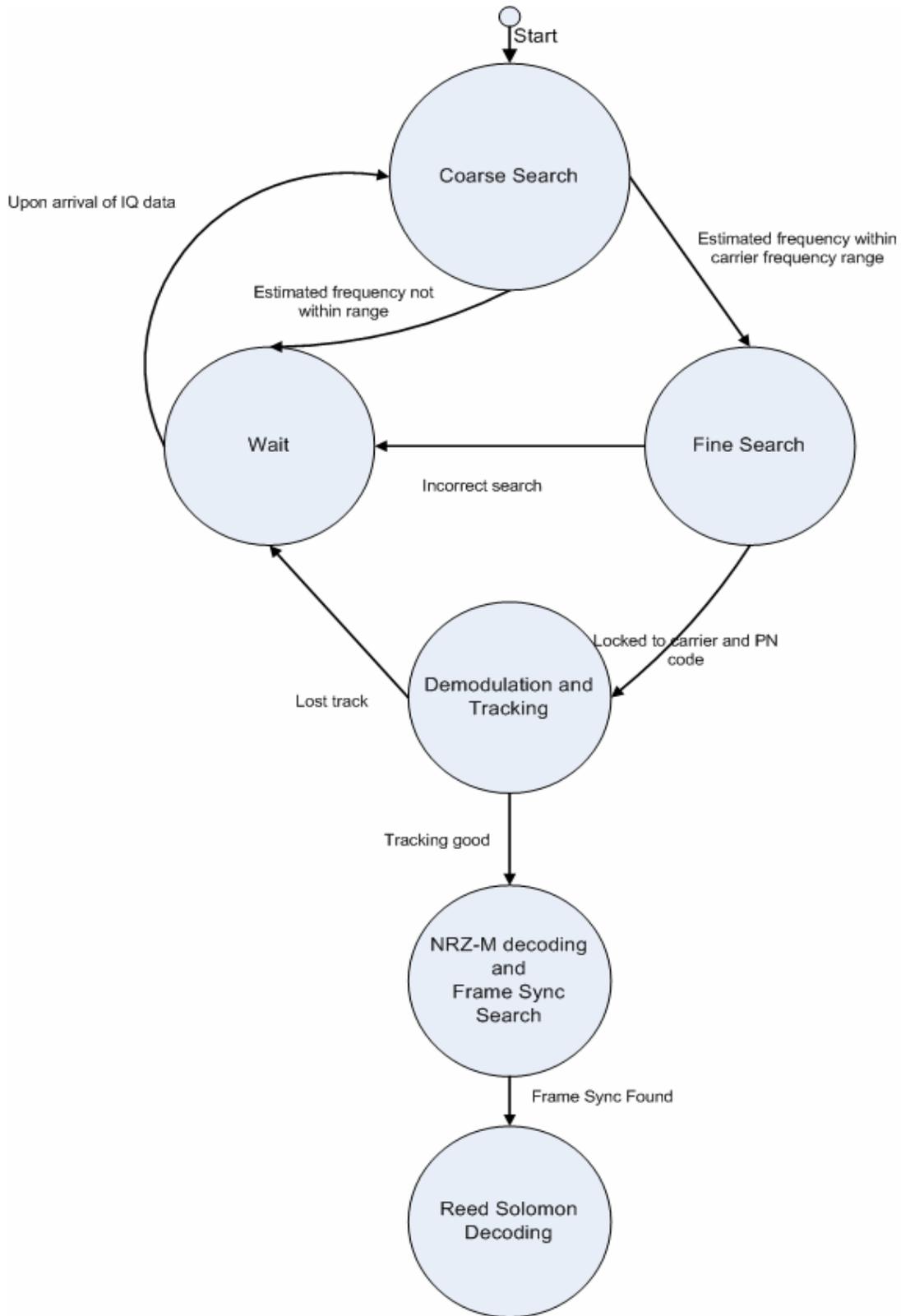
Figure 9: Receiver state diagram

Performance Characteristics

The performance of the DCP Command receiver can be characterized in terms of (a) Frame Error Rate (FER), (b) Interference rejection and sustainability, (c) current consumption, (d) Acquisition and tracking drop times

Efforts have been made to characterize the performance of the DCPCommand receiver in terms of bit energy-to-noise power ratio ($\frac{E_b}{N_0}$). This section will primarily focus on the performance testing procedures, test results and the inferences made from them.

Measurement of probability of frame loss (PFL)

The key performance metric for the DCPCommand receiver is referred to as probability of frame loss (PFL). This is essentially the probability that there will be a lost frame at a certain power level and a lost frame is defined as ANY uncorrectable bit error.

With respect to the architecture of the DCPCommand receiver, a frame of data is a combination of two Reed-Solomon decoded blocks of type RS(255,223), where 223 is the actual number of data bytes in each RS block. Thus, a frame accounts to 446 bytes of data. An error of 1 or more in the 446 data bytes is considered a bad frame in the DCPCommand receiver, and thus being discarded. The probability of frame loss (PFL) is thus defined as probability of receiving a bad frame for a given system input parameter. At present, bit energy-to-noise power ratio ($\frac{E_b}{N_0}$) is considered as a system parameter for evaluating the PFL.

Tests have been performed for evaluating the PFL at various levels of $\frac{E_b}{N_0}$. A transmitted DCPCommand receiver signal is added to a noise signal and fed into the DCPCommand receiver under test. The receiver processes the received signal and sends out the received message data to a Personal Computer (PC) for comparison with the actual message data sent. A spectrum analyzer is used to measure the Carrier-to-Noise Density $\frac{C}{N_0}$, at the beginning and ending of each set of experiment. The DCPCommand receiver also sends out to PC, additional information for further analysis. This information is logged for further analysis.

The following subsections describe the hardware and measurement setup used for the experiment.

Test Setup

Agilent E4438C vector signal generator was used a transmitter, which applies an offset-QPSK modulation with SRRC filter on a band signal with a given carrier frequency and amplitude. An Alpha of 1 is used for the SRRC filter. The band signal is generated on a personal computer (PC) and loaded on to the signal generator. On the PC, a given test message of size 446 bytes is split into two blocks of size 223 bytes. Each block undergoes a Reed-Solomon encoding of type RS(255, 233). The RS encoded data block is NRZ-M encoded and spread spectrum modulated with a predefined PN sequence. Figure 10 depicts the above described procedure.
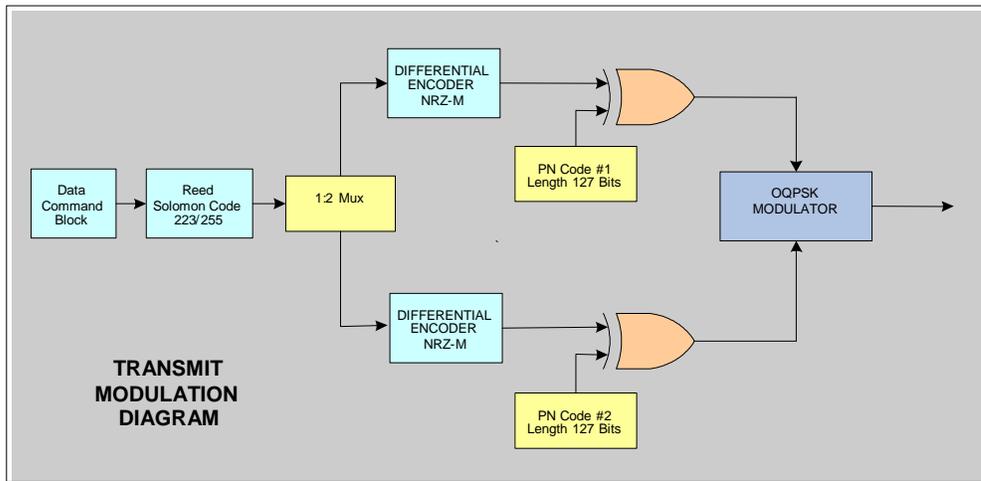
Figure 10: Transmit modulation diagram

A Micronetics NOD-5109 noise generator was used as noise source for combining with the transmit signal. A 20dB attenuators have been placed in each of the signal paths of the pure transmit signal and noise signal paths to maintain proper operating conditions on the Agilent signal generator and noise signal generator. A 3dB power combiner of Mini-Circuits ZFSC-2-1 is used to combine the two signals. Double shielded coaxial cables of RG316-DS with SMA connectors are used as cables in this setup to minimize the signal leakage. The output of the power combiner is then attached to the RF front end of the DCPCommand receiver. Rhode-Schwarz FSU-8 spectrum analyzer was used to measure the $\dfrac{C}{N_0}$, being fed into the DCPCommand receiver. Figure 11 shows the test setup used.

Measurement settings

The Agilent signal generator was made to modulate the transmitted message at a carrier frequency of 468.825MHz and the carrier power level was varied. The Noise generator was set to deliver a constant output noise power level through out the experiments. Variable $\dfrac{C}{N_0}$ was generated by varying the output power level on the Agilent Signal generator. This approach was adapted due to the flexible and reliable output power level control provided by the Agilent signal generator.

The RS FSU-8 spectrum analyzer was set to measure the $\dfrac{C}{N_0}$ with following settings: Detector is of type RMS, Sweep time is 100 S, Frequency Span is 5 kHz, Resolution Bandwidth is 200 Hz, Video Bandwidth is 2 KHz and Preamplifier Enabled. A built-in function to measure the $\dfrac{C}{N_0}$ was used.

Frame Loss computation

The DCPCommand receiver processes the provided signal and sends out the decoded messages on to a PC. A PC program has been written to capture the messages from the receiver and compare it with the actual message sent. The output of the comparison was whether the frame of data sent was decoded correctly or not. If the frame has been decoded incorrectly, an event of frame loss is registered. The ratio of number of bad frames to that of the total

number of frames provides the probability of frame loss. To provide for a reliable ratio, a large number of frames were considered based on the $\dfrac{C}{N_0}$ value injected into the DCPCommand receiver.
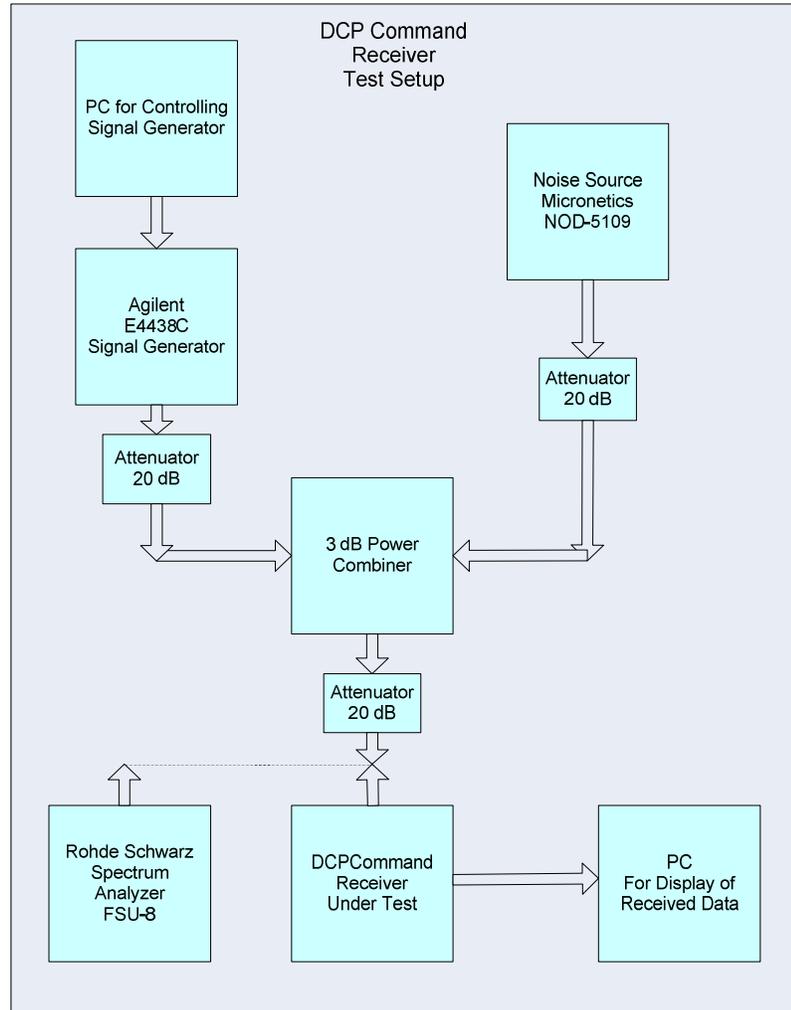
Figure 11: Block Diagram of test setup used to characterize the performance of DCPCommand receiver

To validate the measured PFL values, theoretical PFL values were needed. These values were obtained using the following:

$$PFL = 1 - (1 - P_w)^2 \qquad\qquad (1)$$

where P_w is the probability of bad RS block. A factor of 2 was used to account for the interleaving depth of 2 used in the DCPCommand transmission. The probability of bad RS block for $RS(n,k)$ can be defined as probability of RS errors to be greater than $\dfrac{(n-k)}{2}$ correctable errors.

Experiment Analysis

The measured and theoretical PFL were compared to verify the performance of the DCPCommand receiver. As the comparison of PFL was with respect to $\frac{E_b}{N_0}$, the measured $\frac{C}{N_0}$ is converted to $\frac{E_b}{N_0}$, using the equation (2)

$$\frac{E_b}{N_0} = \frac{C}{N_0} - 10\log_{10}(ThroughputRate) \qquad (2)$$

The *ThroughputRate* is the DCPCommand receiver's Throughput rate, defined as 299.6654 bps.

The measured and theoretical PFL values are tabulated in Table 1.

S. No.	Measured Eb/No (in dB)	Internal Eb/No (in dB)	Measured PFL	Theoretical PFL
1	5.57667273	4.9332	0.888	0.587938995
2	5.76337273	5.1427	0.676348548	0.298254926
3	6.01167273	5.3037	0.423664122	0.071315461
4	6.15834273	5.4992	0.200339559	0.023364518
5	6.35507273	5.7339	0.052264808	0.003895398
6	6.54167273	5.9373	0.013544018	0.000528799
7	6.71867273	6.1526	2.36E-03	6.14522E-05
8	7.02167273	6.3569	1.36E-04	8.80255E-07

Table 1: Measured and Theoretical probability of frame loss (PFL) for various measured bit energy-to-noise ratios. The table also reports the internal Eb/No reported by the DCPCommand receiver.

The plot comparing the above values can be seen in Figure 12. It can be seen that measured (blue) and Theoretical PFL (green) are off by a factor of 0.3dB. This factor accounts for the implementation loss involved, which arises due to the fixed-point implementation of the signal processing filters and algorithms.

The plot also shows the internal $\frac{E_b}{N_0}$ computed by the DCPCommand receiver from the data being processed. This computation seems to have an offset of 0.6dB with respect to the measured $\frac{E_b}{N_0}$. This offset can be introduced into the DCPCommand receiver to report the appropriate $\frac{E_b}{N_0}$ to the user, thus removing the need for an expensive spectrum Analyzer to measure the $\frac{E_b}{N_0}$ in the field.

Further analysis led to another observation made during the experimentation was regarding the distribution of Reed-Solomon correctable errors at various $\frac{E_b}{N_0}$ values. Figure 13 shows the details. It can be noticed that as the $\frac{E_b}{N_0}$ increased, the distribution curve skews towards left, providing better receiver performance. This gives further evidence as to the fact that the Reed Solomon code is operating as designed.
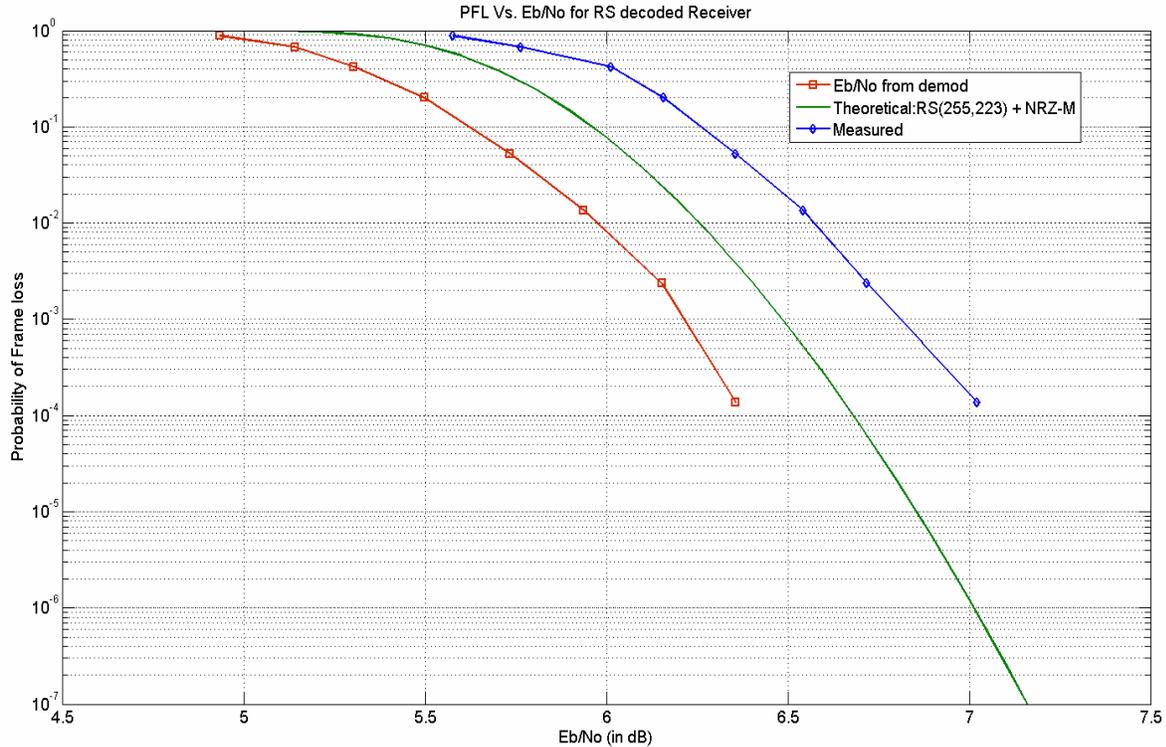
Figure 12: Plot comparing the PFL values obtained from measurement and theoretical calculations with respect to the measured Eb/N0 values. The line "Eb/No from demod" plots the measured PFL values with respect to the Eb/No reported by the DCPCommand receiver
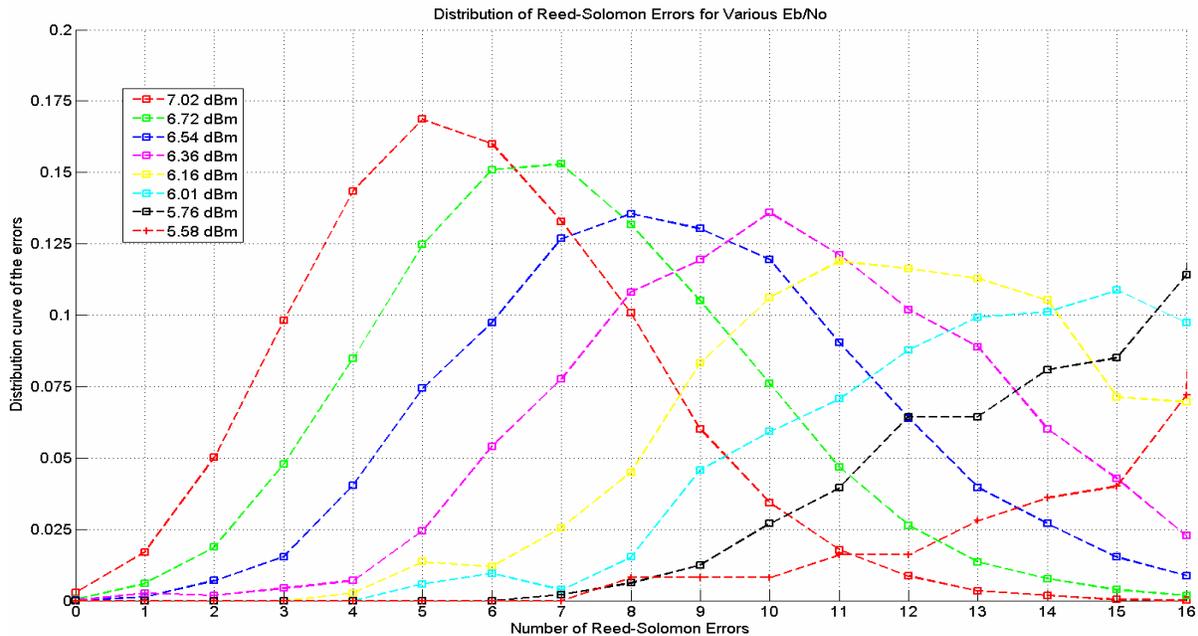
Figure 13: Normalized histogram of the Reed-Solomon Errors for various $\dfrac{E_b}{N_0}$ values.

The Figure 14 represents the net performance of the prototype system as compared to the 'perfect' theoretical case and is considered the definitive chart in performance measurement.   The horizontal shift represents the implementation loss and currently slightly less than 0.,5 dB implementation loss is indicated. The expected implementation loss is around 1.5 dB. This may reflect some measurement error with respect to using the spectrum analyzer or in making the noise measurements. This represents performance that is just short of fantastic.
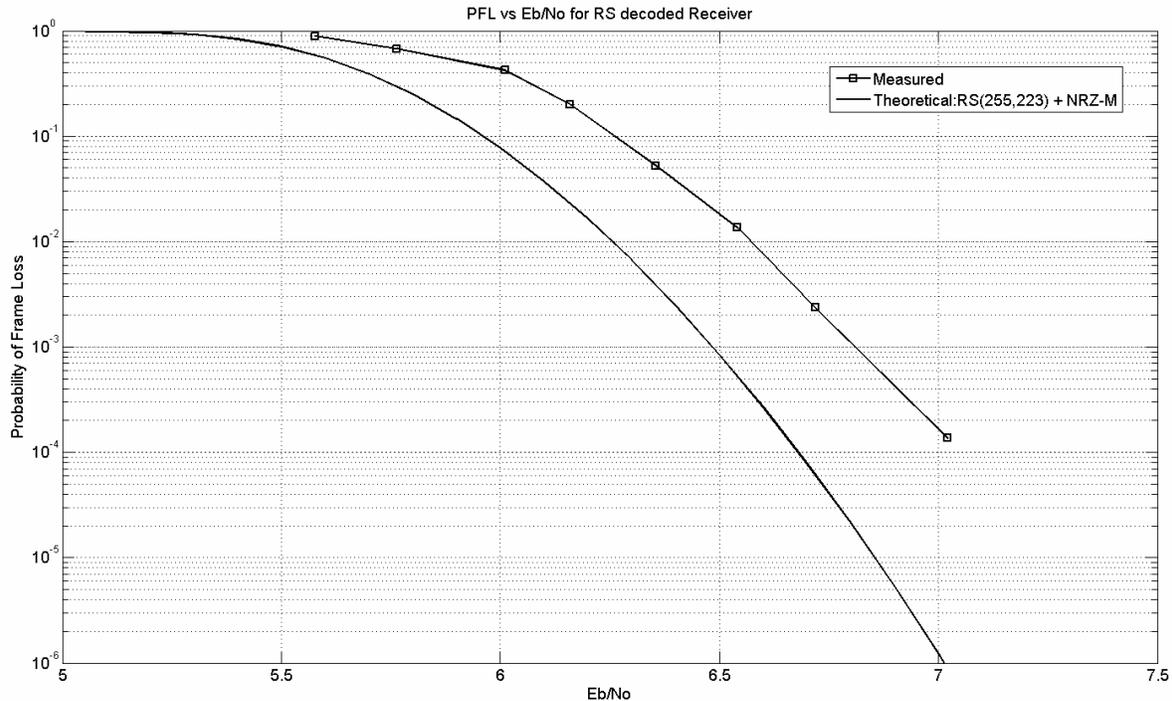
Figure 14: Simplified Plot comparing the measured PFL values and the theoretical PFL performance calculation.

The above performance experiment to verifies that performance of the DCPCommand receiver with respect to PFL was able to demonstrate that the DCPCommand receiver has excellent performance capability, matching with the theoretical performance with a very low implementation loss. The internal $\frac{E_b}{N_0}$ from the receiver (self measurement) also agrees with the external $\frac{E_b}{N_0}$ measurement with an offset value.

Interference rejection and sustainability

Interference tests have been performed to verify the operation of the receiver. For this, the incoming IQ signal has been set at 468.825MHz and at a power level of -108dBm. An interference signal has been placed at an offset frequency from the IQ signal frequency. Two situations were considered. (1) interference power levels at which the receiver operates without losing track, and (2) interference power levels at which the receiver loses carrier track and enters coarse search mode.
The results of the interference test can be seen in the Figure 15 below. Interferer was placed at various offset frequencies and reception and acquiring conditions were evaluated. The interference test results were satisfactory.
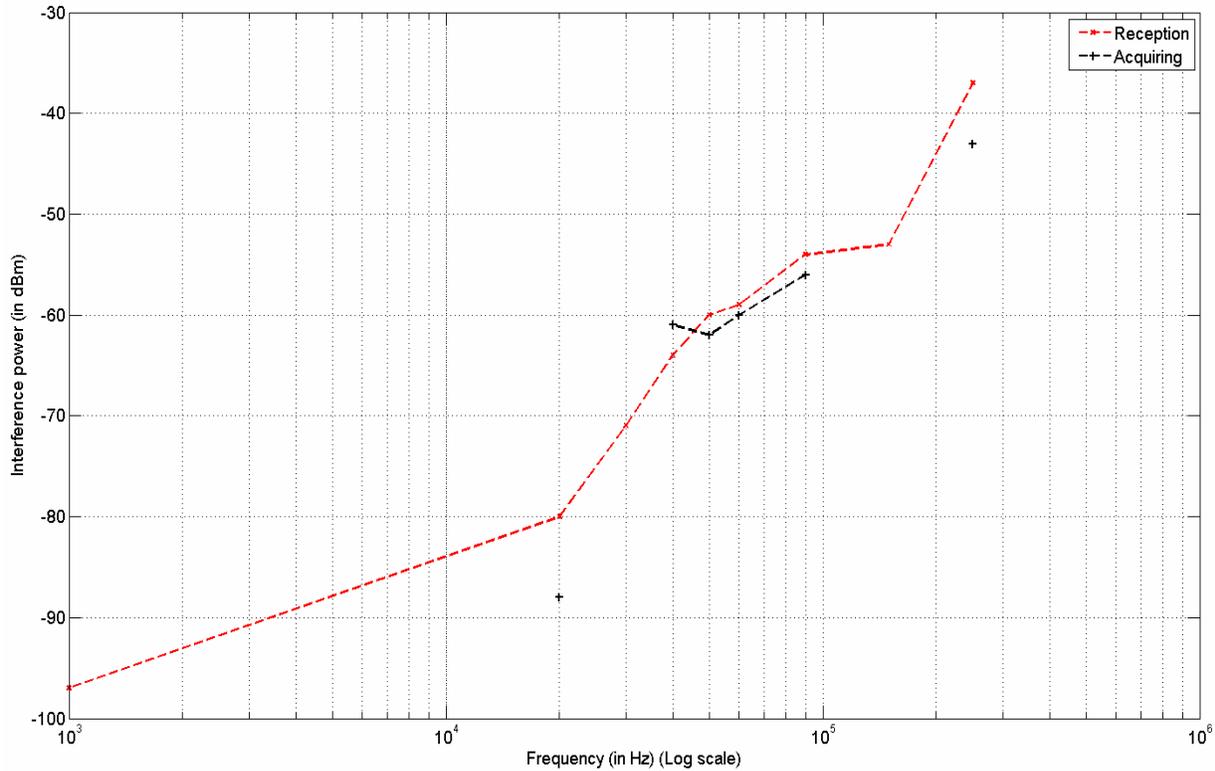
Figure 15: Interference test results. The IQ signal has been set at -108dBm. The condition "reception" means that the interference power level at which receiver is able to operate without losing carrier lock. The condition "acquiring" means that the interference power level at which the receiver loses PN and carrier track and starts searching for the signal.

In a different interference test pattern, a Family Radio Service (FRS) signal at 467.7125MHz is used as an interferer. The receiver was able to sustain an interference power level up to -40dBm.

Current Consumption

One of the primary goals of the DCPCommand receiver was to have a low power design. The current consumption characteristics of the DCPCommand receiver are acquired by connecting a ammeter in series to the power supply of the DCPCommand receiver. Thus, the effective current consumption of the DCPCommand receiver is very satisfactory.

The original current consumption for the system was predicted as follows:

Part	Current Consumption
RF Front End	200 mW (17 ma @ 12 Volts)
TMS DSP Processor	100 mW
TOTAL SYSTEM	300 mW (25 ma @12 Volts)

Results from the prototype:

Part	Current Consumption
RF Front End	480 mW (40 ma @ 12 Volts)
TMS DSP Processor	528mW (44 ma @ 12 Volts)
TOTAL SYSTEM	1008 mW (84 ma @12 Volts)

Note that this represents the system running at full power. When duty cycle averaging is used, the power consumption is reduced significantly.

Results from the prototype using 50 % duty cycle averaging:

Part	Current Consumption
RF Front End	240 mW (20 ma @ 12 Volts)
TMS DSP Processor	264mW (22 ma @ 12 Volts)
TOTAL SYSTEM	504 mW (42 ma @12 Volts)

The above results are for the entire command receiver. This estimate is based on the DSP running continuously. The use of low duty cycle for the receiver 'on' time will allow the power consumption to be reduced even further. This is only an estimate and will give us a baseline in comparison to other approaches.

Acquisition and Tracking times

Acquisition test

In this performance test, the receiver was provided with a low C/No signal initially. The C/No was gradually increased, until the receiver acquires a signal. Time between the start of the receiver from a default state to the time the decoded message is transmitted out was measured for different values of C/No signal. The Figure 16 below shows the time taken by the receiver for various C/No.
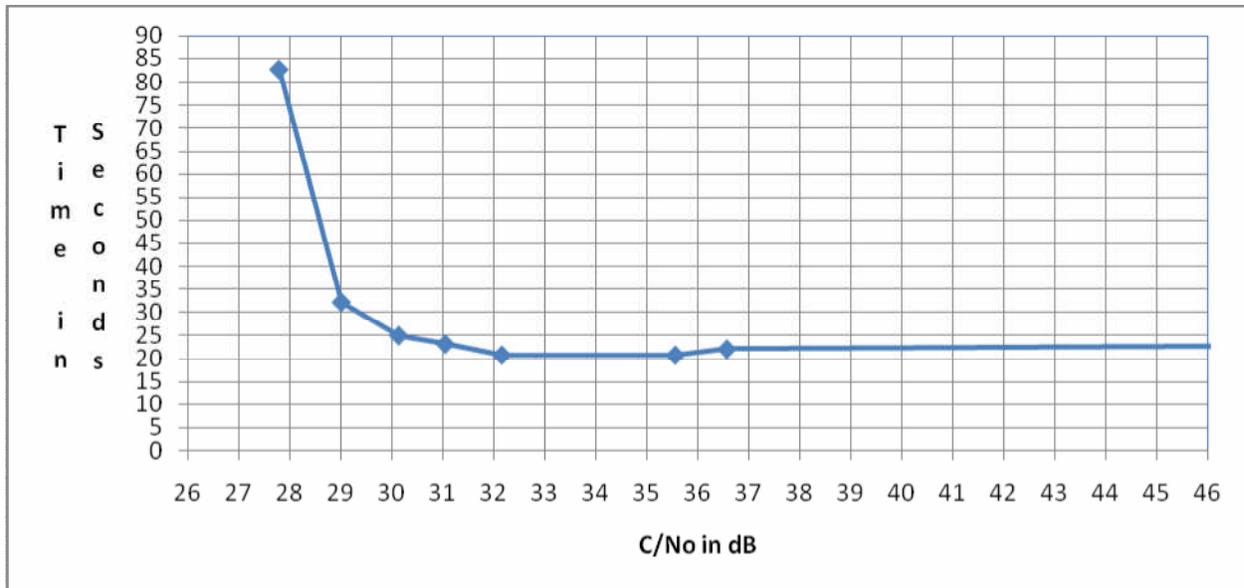
Figure 16: Acquisition time of the DCPCommand receiver for various C/No values. As the C/No decreases, the DCPCommand receiver takes longer time to search and decode the message. For optimal C/No, the DCPCommand receiver has an acquisition time of 23 seconds.

It can be observed that as the C/No value decreases, the minimum time taken to search and decode the messages increases. For optimal C/No, the DCPCommand receiver has an acquisition time of 23 seconds.

Tracking drop test

In this test, the receiver was made to run freely at a C/No value at which the receiver can acquire and decode messages. While observing the decoded messages, the carrier power level was decreased, resulting in drop of C/No. The C/No, at which the receiver loses its tracking and enters and stays in search mode, was observed. A value of -30.94 dBm-Hz was observed representing a very good low level signal dropout condition.

The excellent performance of the DCPCommand receiver with respect to acquisition and tracking drop tests can be attributed to the software written. The software implementation has multiple buffering schemes and robust tracking loops to track the signals even at low signal levels and also to handle short outages in the signal reception.

GENERAL FEATURES and COMMENTS

The new data block structure will bring two-way communications to a DCP with the ability to send up to 64KBytes of data to a station.

The command link (initially) shall consist of two channels (1 per satellite) at a downlink frequency centered at 468.823 MHz. Future expansion to a secondary channel on each satellite is an option.

1) Each channel shall operate at a physical layer symbol rate of 342.6667 Baud. The efficiency on the link is 84.8% making an effective throughput of 299.6654 bps. (approx 300 bps)

2) When future satellites with more RF downlink power are operational, either an additional channel can be added because of its higher margins and the spread spectrum bandwidth utilization, or the extra EIRP kept for increased interference rejection.

3) Each channel shall transmit a fixed length block of 514 bytes including synchronization patterns, data and error detection/correction codes, this leads to 444 bytes of user data per frame.

4) The block rate is (514*8/342.666 symbols/sec = 12.000 seconds => 5 blocks per minute.

5) The entire block must be received in order to validate it and process it.

6) Each block can hold up to 444bytes/6bytes/command = 74 (short) commands per block, for a capacity of 6.166 commands per second, leading to a total of 532.8k command/day. Longer commands reduce the capacity.

7) The command format allows for group and individual addresses.
Receivers will be able to belong to up to 10 groups. Each user will be given a series of group numbers to use.

8) The command format supports command authentication by combining the time, ID and secret key. If the secret key for a station is not defined, authentication is not performed.

9) The protocol supports predefined commands for common maintenance functions.

10) The link supports a "file transfer" command that allows the transfer of up to 64 KBytes of data.

11) The link supports user defined commands.

12) The command can request the DCP to reply to the command. Replies are made on normal DCP uplink channels set aside for this purpose. The reply request includes specific information on when to transmit and what channel to use allowing this to be controlled remotely. Note that the latency in the reply can be anywhere from (conceivably) directly after the command has been received to several minutes or hours depending on when the open channel space is available for reply.

13) Most commands (except file transfer) must fit inside one frame, otherwise the frame is padded with filler and the command sent in the available next frame. This, together with the 'atomic' nature of certain command functions (e.g. channel is always specified along with schedule information), ensures there will not be mistakes in operational function changes.

14) The capability exists for a command to instruct the receiver to enable its second channel and receive configuration or setup downloads on the secondary channel. Once that is complete, the second channel may be shut off to conserve power.

Future Anti-Interference Enhancements

Our base line design is for a DS-SS system with a processing gain of around 21dB, and a link margin of at least 3dB. These allow for the rejection of a modest amount of in-band interference by virtue of the spread-spectrum system's operation. Unfortunately, the actual space-ground link power is very small at the Earth's surface, so in absolute terms the tolerable in-band interference limit is not very large.

We can imagine a method of dealing with narrow-band interference (e.g. low deviation FM audio link, spurious from digital clock system, etc) where the input filtering is adaptive to reduce signals that are narrow compared to the expected DS-SS spectrum. Such a method requires complex signal analysis and adaptive filtering, most likely implemented in the frequency domain via the FFT, and would greatly increase the processing complexity. Therefore we consider that a good choice of implementation method should be one that allows for ease of design change, and that complex processing steps can be implemented.

Time Code (System Clock) Synchronization

The proposed system has the ability to provide a very accurate time base that is provided in the header as previously defined. However, the time provided in the data frame will be offset to coincide with the edge of a block, either that block or the next block to give time for the overhead to be processed on the message frame.

This provides the ability to have a uniform time source or at least a backup source of time for remote transmitters as GPS is still the favored technique to obtain a time synchronization for a system.

There are several benefits as well as issues associated with Time code synchronization:

- Overhead necessary to have NBS or other GPS time source linked to the uplink signal.
- Discrepancy in time of RF propagation based on location on earth with respect to satellite. (Path Delay variations) Corrections are possible using GPS based location information associated with DCPs.
- Defining the Time code reference point in the data, i.e., the time is given with the time calculated to be at the end of the block, etc.
- Using the Chip Rate itself to serve as an accurate source of defining a time base that is not synchronized exactly due to the geographical errors related to geostationary satellite communication. This highly accurate rate may be used to calibrate an internal reference frequency if desired in the time base portion of the circuitry.

The time information imbedded in the stream of data will clearly be valuable for setting the day, date, time etc. Decisions on how NESDIS implements this format as well as path delay compensation will ultimately determine whether this is a 1 second, 100 ms, or 10 ms accurate type system.

The system also has the ability for the receiver to know the location that it is installed and calculate signal delays to the satellite yielding very accurate time results. Also a mechanism shall be in place to notify the leap second many months in advance to prevent any problems with missing the information. This technique will simulate what the GPS system does to notify leap seconds.

Command Receiver Frequency Discipline

The system also has the capability to use the received chip rate from the receiver to serve as a source for an accurate frequency reference for the receiver system. This capability would ultimately allow for any ageing or temperature related oscillator effects to be removed from the system. This would also provide the system with a faster time locking to the signal ultimately translating into lower power consumption. This potentially would assist in keeping

the cost of the system down by using less expensive oscillators in the receiver.   The drawback to this concept would be that the system would take a longer time to acquire the signal for the first time and determine the frequency error, but from that point forward, the system would have significantly faster times to lock over any temperature condition given routine updating of the frequency error.

An alternate method for frequency disciplining would be to use a GPS receiver and the 1 Hz output it provides instead of using the received chip rate to calculate the frequency error.

In order to achieve frequency discipline, several of the following would be required:

- A 1 Hz (or other) output source from a GPS receiver. This receiver may be either included with the command receiver or it may be an output from a certified transmitter that has the GPS built in. A provision for its interface would be required. –or-
- Design of the Command receiver to use the received chip rate to discipline its oscillators.
- Wallops Command station would have the requirement to synchronize the chip rate to a NBS or equivalent frequency reference source.

Advantages

- Reduced search time for frequency lock will improve the robustness of the link with faster time to lock.
- Lower cost oscillators reducing the cost of the receiver.

Disadvantages

- Requires a GPS receiver to be located in any of the following:
    a) in a certified transmitter that is co-located with an 'add on' receiver.
    b) the same unit if this is a 'combined' receiver and transmitter
    c) located in the command receiver independent of any transmitter.

- System will need to operate for longer times that what may be necessary if not performing a discipline. A typical discipline time may be up to 2 or 3 minutes if done on an hourly basis. In some cases, the transmitter will already have the GPS receiver on for the same discipline purposes and may therefore that 'on time' may be shared creating no or minimal additional power consumption.

Wallops Island Testing

First Test

In November of 2008, a demonstration of the receiver operation was done using the existing Wallops provided Helix Antenna which is a very high gain antenna. This test served the purpose of verifying that the signal was compatible with the satellite transponder and that the system will operate. A demonstration was done for the STWIG group.

Second Test

In June of 2009, a second visit to Wallops Island was made to test the receivers in the field with real antenna that would likely be used with the product.   Both of these antenna were prototype antenna but they reflect the type performance that is likely to be observed with each type.
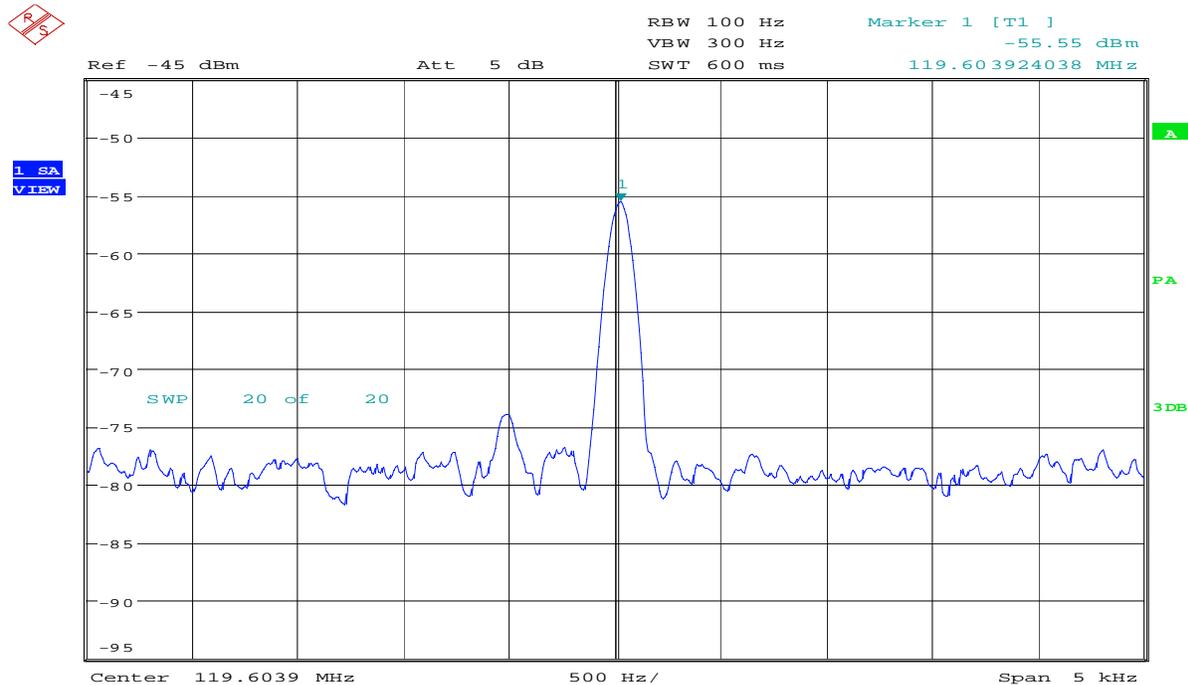
Figure 17: Snapshot of spectrum of carrier signal acquired through helix antenna

1) Test with Helix antenna. The carrier signal was measured from the satellite as received through the antenna. The screen shot below is an example of the signal strength received. Notice the signal located one box lower in frequency that is barely visible. That signal is from the West satellite but because the antenna is directional and pointing at the East satellite, the West signal is much lower.

The Figure 17 shows that C/No= -55.55 – (- 97.48) = 41.93 at the 119.6 MHz IF. (Note that the noise floor of the analyzer is >>30 dB lower yielding insignificant errors.)   All data was received without error.

Performance of helix antenna

The measured C/No is about 41.93 dB. The required C/No is approx 33.5 dB. **Thus a margin of 8.43 dB**

2) Test with a Quadrifilar Helix antenna: Using an Omni style antenna in this example shows that the overall gain is reduced but secondly, that both West and East signals are visible due to the omni pattern of the antenna.

The Figure 18 shows that the C/No = 58.35 – 97.10 = 38.75 dB   (No correction necessary for spectrum analyzer.)

Performance with Omni Directional antenna:
         The measured C/No is about 38.75 dB the required C/No is approx 33.5 dB.   All data was received without parity. **Thus, a margin of 5.25dB.**
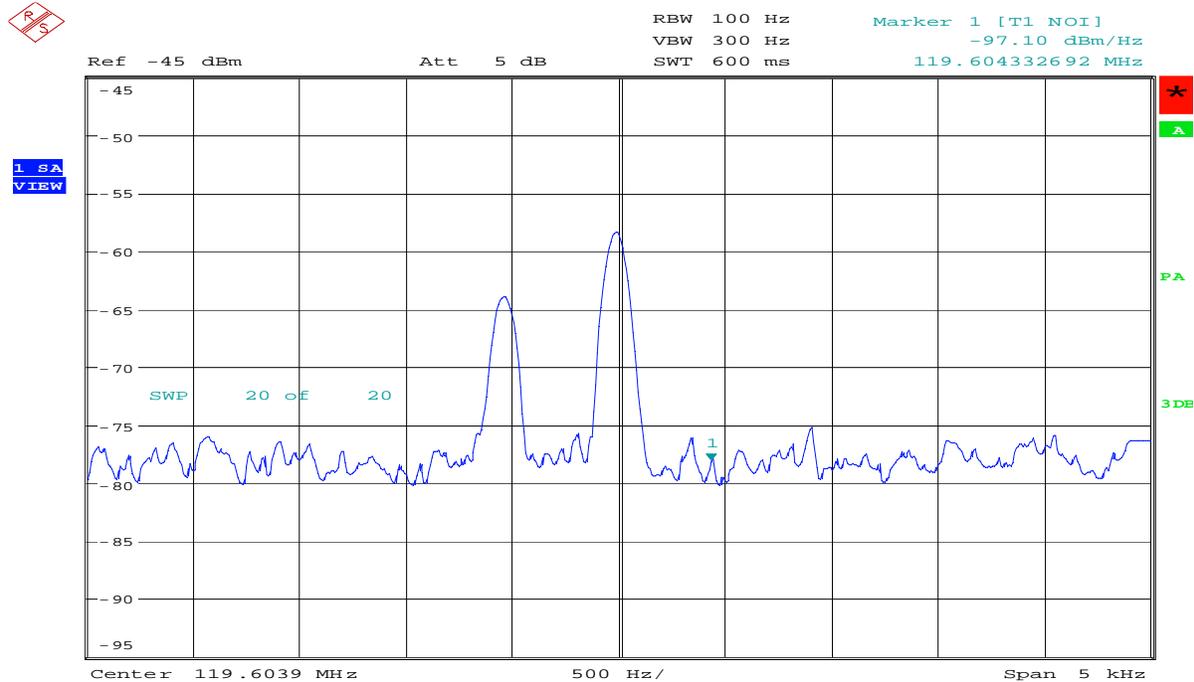
Figure 18: Snapshot of spectrum of carrier signal acquired through omni directional antenna

RESULTS

The significance of the tests indicates that there may be sufficient signal strength on the satellite to permit the simultaneous operation of 2 channels at one time. This is one of the KEY significant findings from the test. Having a second channel is important for the reason that the system may be able to support DCP site downloads that could now include site setup files, etc. Sutron looks forward to performing further tests once Wallops Island gets a test system in place.

CONCLUSIONS

The main conclusion to this project is that Sutron has proved that the proposed CDMA technique will be a robust, reliable, and highly desirable solution for bringing the DCP Command to market. The on-the-fly reconfigurable DCPCommand receiver shall provide more controllability and adaptability. The DCPCommand receiver performance has also demonstrated that it can be expanded to multiple channel usage. It offers all the advantages with very few if any disadvantages.

FINAL RECOMMENDATION

In quick summary:

- Proceed with experimental Wallops Island Uplink DCPCommand facility to permit the testing of the prototype receivers.
- Get experimental receivers into the customer's hands in the field. This will help prove to the key users that the system works as advertised.

HOURS EXPENDED

Here is a summary of the hours spent on the project over the entire Phase 2 SBIR:

Name of Individual	Title	Hours Expended
Dan Farrell	VP	44
Chris Buchner	Principle Investigator	1367
Siva Telasula	Engineer	1781
Paul Crawford	Consultant	577
Adi Rustanbegovic	Software Engineer	7
Tim McDonald	PCB Cad Designer	237

APPENDIX A: SYSTEM SPECIFICATIONS and DIAGRAMS

The specifications for the National Oceanic and Atmospheric (NOAA) Data Collection Platform Interrogate (DCPCOMMAND) service are recommended below. These specifications are for a Direct Sequence Spread Spectrum CDMA link:

	DESCRIPTION	SPECIFICATION
1	Frequency Band	468.799 MHz to 468.847 MHz
2	Available Modulation 3dB Bandwidth	48.0 KHz
3	Center Frequency	468.823 MHz +/- TBD
4	(DS-SS) Direct Sequence Spread Spectrum Modulation	Offset QPSK
5	User Channel Multiplexing	CDMA
6	Encoding Inner Layer	Reed Solomon (255/223) I=2 interleaved code blocks.
7	Encoding Outer Layer	Differential Encoding NRZ-M
8	Net Link Data Rate with R/S Overhead	342.6667 bps
9	Throughput	299.6654 bps
10	RF Symbol Rate	171.3333 bps
11	Chip Rate	21.7593333 KHz
12	Occupied Bandwidth	43.5186667 KHz
13	PN Code Length	127
14	Processing Gain	21.04 dB
15	Transmit Filter	RRC (alpha = 1.0)
	CDMA PN code sequences **	
	GOES East I	B6 24 89 C7 85 0E 65 F3 6E 69 E7 AA B8 1B 61 12
	GOES East Q	07 EA 31 8B 90 67 4C 17 04 76 3A 17 AE 44 71 20
	GOES West A	86 71 2D 60 14 A6 1A 85 9A 30 9B EA 75 95 14 D0
16	GOES West B	67 41 78 C4 B3 37 B2 FA EC C4 C2 96 35 58 9A A4
17	Frame Sync Characters (CCSDS)	1ACFFC1D
18	Frame Length	12.0 seconds
19	Frames per minute	5
20	Error Handling	Retries & acknowledgements
21	Receiver Sensitivity (est)	-130 dBm
22	Recommended Antenna	3 dB Omni or 6 dB helical
23	Recommended Power Consumption	< 25 ma @12 V

** The representation below is a 16 x 8 byte representation. The LSB, or right most character has been stuffed with '0' and will be stripped or disregarded during implementation.

APPENDIX B: DCP-COMMAND BLOCK DIAGRAM

ENCODING and MODULATION
SEQUENCE
(WALLOPS ISLAND)

| Data | REED SOLOMON ENCODING | DIFFERENTIAL ENCODING NRZ-M | CDMA PN SPREADING CODE | RF MODULATION TX RRC Filtering OQPSK |

RF LINK

DEMODULATION and DECODING
SEQUENCE
DCPCOMMAND RECEIVER

| DATA | REED SOLOMON DECODING | DIFFERENTIAL DECODING NRZ-M | CDMA PN DESPREADING | RF DEMODULATION Receive RRC Filtering OQPSK |
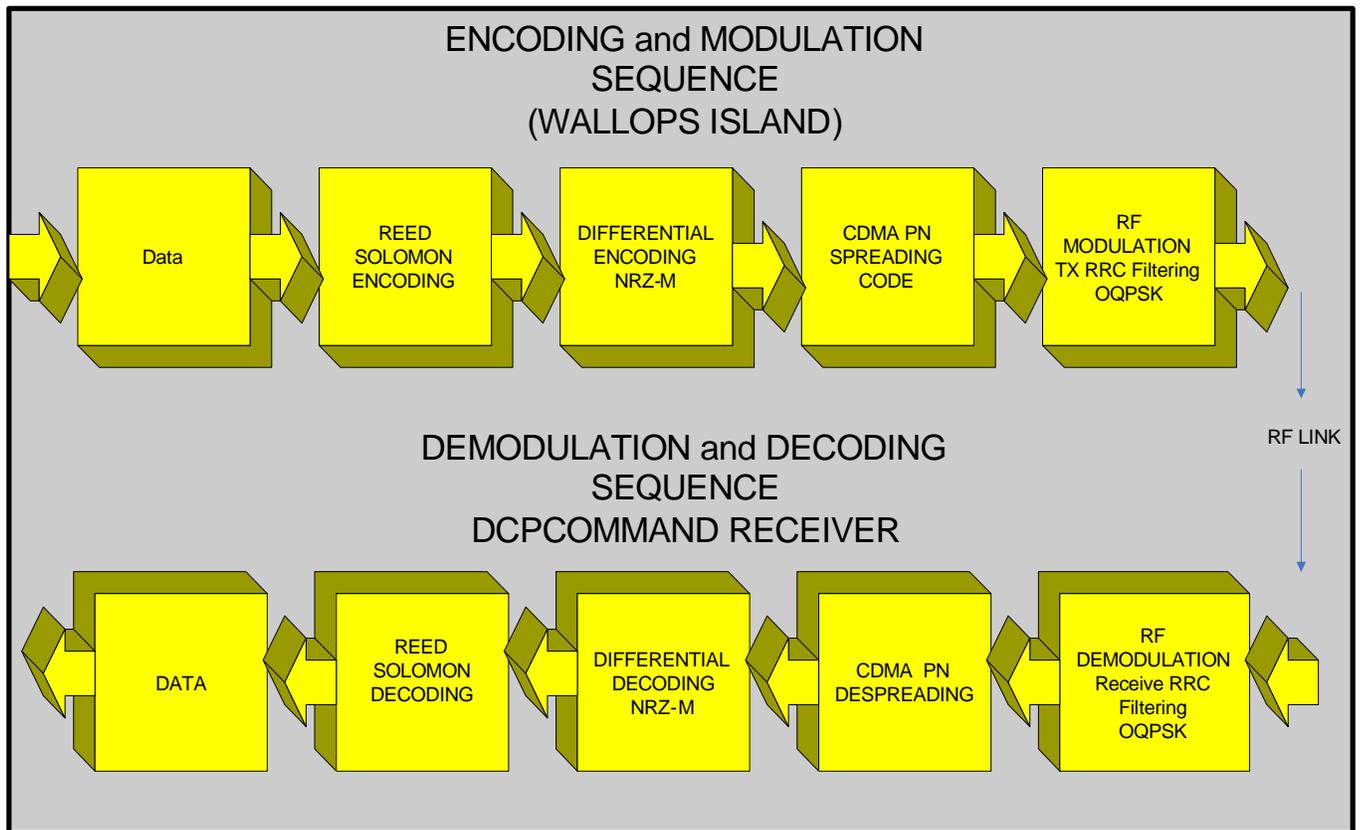
APPENDIX C: DATA PACKET PROTOCOL DESIGN

The GOES DCP COMMAND will utilize the recommended data format specified by the Consultative Committee for Space Data Systems (CCSDS). The overall structure is based on the standard Reed Solomon packet length as shown below:

DCPCommand Frame Format

RS (255,223)
Interleave Depth = 2

This is a Block operation. After 446 bytes are loaded into the 2 RS encoder blocks, the RS Overhead bits are then caclulated. Output sequence begins only after the overhead is completed. New bytes are not loaded into the RS blocks until the blocks have completely emptied. Operation is continuous.

2 x 223 BYTES (446 BYTES)
3568 BITS

DATA BLOCK (446 bytes)

REED SOLOMON BLOCK #1 (255 bytes)

DATA Block 'A' (DA) (223 bytes) — RS Overhead 'A' (RSA) (32 bytes)

DATA Block 'B' (DB) (223 bytes) — RS Overhead 'B' (RSA) (32 bytes)

REED SOLOMON BLOCK #2 (255 bytes)

SYNC BITS 1ACFFC1D

DA 1 | DA 2 | ... | DA 223 | RSA 1 | RSA 2 | ... | RSA 32
DB 1 | DB 2 | ... | DB 223 | RSB 1 | RSB 2 | ... | RSB 32

4 Bytes — 446 Bytes — 64 Bytes

514 BYTES
4112 BITS

COMPLETE TRANSMITTED FRAME
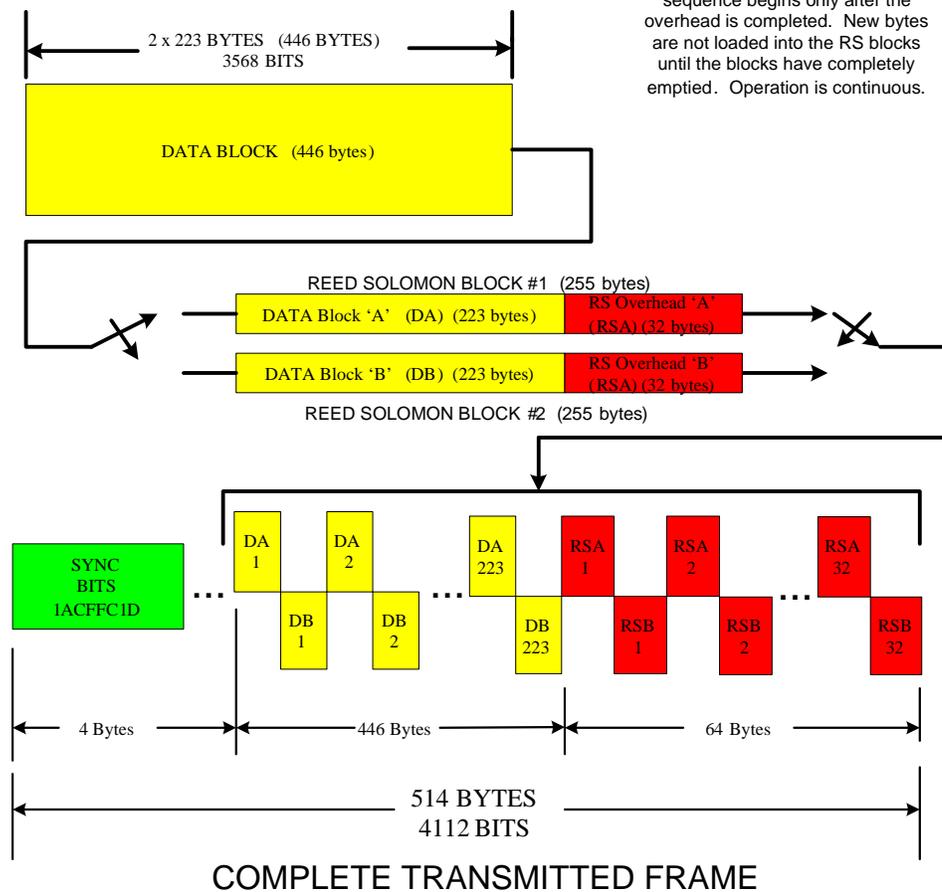
The bottom portion of the diagram explains how the interleaving of the data block(s) and RS overhead is accomplished. Note that the sync bits are NOT part of the interleaving process. In the above example, the RS calculations on Block 1 are calculated independently of Block 2.

APPENDIX D: DOWNLINK MESSAGE PACKET DEFINITION

General Structure

Repeat the following block with no gaps between blocks.

Complete Block Structure:

Name	Length (bytes)	Description
CCSDS Sync Word	4 bytes	Sync pattern identifying start of block
RS Block Data	446 bytes	Fixed length block of data 2 frames interleaved of 223 bytes each
RS Correction Bits	64 bytes	Reed/Solomon error correcting code 32 bytes each frame for total 64 bytes
TOTAL LENGTH	514 bytes	2 RS blocks = 510 bytes + 4 byte Sync

CCSDS Sync Word :

Name	Length (bytes)	Format	Description
Sync Word	4 bytes	4 byte CCSDS	1ACFFC1D (Hex)

RS Block Data ::= Header + Command Data

Header :

Name	Length (bits)	Format	Description
Time	8	1 byte	Minutes past xxxx Date (UTC time)
AddLeap	1		1=add a leap second at 0 UTC
SubLeap	1		1=subtract a leap second at 0 UTC
HeaderType	6	binary	'01'H Type 1 '02'H Type 2
TOTAL LENGTH	16 (2 bytes)		

Type 1 Message :== { command }
Message consists of 1 or more commands to fill the block

Command Data :

Name	Length (bits)	Format	Description
Grp/Addr	1	binary	1=group 0=address
ID	21	binary	21 bit destination group or address
Command	8	binary	Predefined commands, see below
Authentication	16	binary	Use ID and TIME and key to authenticate command
ReplyRqst	1	binary	0=no reply 1=reply
Spare	1	Binary	0
Basic Command Total Length	48 (6 bytes)		

Command Extension :

Name	Length (bits)	Format	Description
Undefined	1	binary	0
[replyslot]	40 + ??	see description	2 bits baud: '00'x=100 '01'x=300 '10'x=1200 '11'x=future use 10 bits channel: binary channel number 18 bits time: seconds into day? xx bits reply length
[Cvalues]	variable	see commands	Command specific data
Command Extension Total Length	Increments of 8 bits (1 byte)		

This permits exactly 74 commands at a minimum command length of 6 bytes for each command. That number can be reduced if long commands are transmitted.

APPENDIX E: LINK BUDGET

GOES DCPI Satellite Link Budget

Boltzmann's constant	1.38E-23	
Bit Rate	306.1	User rate without frame overhead
Downlink frequency (MHz)	468.8125	
Downlink wavelength (m)	0.6399	
Path length (m)	41679000	
Spreading factor [processing gain dB]	127	21.04
FEC coder rate	0.875	
Symbol Rate	350.000	Before spreading / modulation
FEC required Eb/No for BER=1E-6 (dB)	7.0	
Chip rate	44450	
Tx filter RRC 'alpha' parameter	1.0	
Occupied TX bandwidth (kHz)	88.90	BPSK
Occupied TX bandwidth (kHz)	44.45	QPSK

Specification Link	Wallops to Spacecraft	Spacecraft to DCPI Receiver 468.8225 MHz							
	UPLINK	GOES SERIES I/M				GOES SERIES N/O/P			
# of Active Channels on BOTH spacecraft	2034.9 MHz	1	1	2	2	1	1	2	2
		LAND	BUOY	LAND	BUOY	LAND	BUOY	LAND	BUOY
		Yagi	Omni	Yagi	Omni	Yagi	Omni	Yagi	Omni
Tx Power (dBm)	40.00	35	35	35	35				
Tx Line Loss (dB)	0.00	1.3	1.3	1.3	1.3	GOES-N EIRP			
Tx Antenna Gain (dB)	0.00	11.1	11.1	11.1	11.1	provided by Peter Wolner			
EIRP = (dBm)	85.70	44.80	44.80	44.80	44.80	47.00	47.00	47.00	47.00
Tx Power Share Loss (dB)	0.00	0.00	0.00	3.01	3.01	0.00	0.00	3.01	3.01
Tx Antenna Pointing Loss (dB)	0.50								
Net EIRP	85.70	44.80	44.80	41.79	41.79	47.00	47.00	43.99	43.99
Free Space Loss (dB)	191.00	178.26	178.26	178.26	178.26	178.26	178.26	178.26	178.26
Polarization Loss (dB)	0.20	0.20	0.50	0.20	0.50	0.20	0.50	0.20	0.50
Rx Power Ref to Isotrope (dBm)	-106.00	-133.66	-133.96	-136.67	-136.97	-131.46	-131.76	-134.47	-134.77
Rx Antenna Gain (dB)		10.50	3.00	10.50	3.00	10.50	3.00	10.50	3.00
Rx Line Loss (dB, assumed at 290K)		1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
Rx Pwr (dBm)		-123.16	-130.96	-126.17	-133.97	-120.96	-128.76	-123.97	-131.77
Antenna Temp K		145.00	165.00	145.00	165.00	145.00	165.00	145.00	165.00
Receiver Noise Figure (dB)		4.00	4.00	4.00	4.00	4.00	4.00	4.00	4.00
Receiver & line noise figure (dB)		5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00
Receiver Temp K (ref. to antenna)		627.06	627.06	627.06	627.06	627.06	627.06	627.06	627.06
System Temp K (ref. to antenna)		772.06	792.06	772.06	792.06	772.06	792.06	772.06	792.06
Thermal Noise Pwr at Receiver (dBm/Hz)		-169.72	-169.61	-169.72	-169.61	-169.72	-169.61	-169.72	-169.61
Rx System G/T dB/K	-25.00	-18.38	-25.99	-18.38	-25.99	-18.38	-25.99	-18.38	-25.99
Rx C/No (dB-Hz)	67.60	46.56	38.65	43.55	35.64	48.76	40.85	45.75	37.84
306 BPS DS-CDMA									
Turnaround C/No		46.53	38.65	43.54	35.64	48.71	40.84	45.72	37.84
Available Eb/No (dB)		20.17	12.29	17.18	9.28	22.35	14.48	19.37	11.48
Demodulation & despreding loss (BPSK/DSSS)		1.50	1.50	1.50	1.50	1.50	1.50	1.50	1.50
Useful Eb/No (dB)		18.67	10.79	15.68	7.78	20.85	12.98	17.87	9.98
Useful Eb/No (numeric)		73.62	11.99	36.96	6.00	121.56	19.88	61.17	9.95
Eb/No including all other CDMA signals (dB)		16.68	10.40	12.95	7.20	17.93	12.35	13.98	9.06
Desired margin (dB)		3.00	3.00	3.00	3.00	3.00	3.00	3.00	3.00
Required Eb/No (dB)		10.00	10.00	10.00	10.00	10.00	10.00	10.00	10.00
Excess Margin (dB)		6.68	0.40	2.95	-2.80	7.93	2.35	3.98	-0.94
Thermal Noise (W in RX BW)		3.73E-18	3.83E-18	3.73E-18	3.83E-18	3.73E-18	3.83E-18	3.73E-18	3.83E-18
Allowable noise (W in RX BW due to total margin)		3.47E-17	8.37E-18	1.47E-17	4.01E-18	4.62E-17	1.31E-17	1.86E-17	6.15E-18
Max interference (W)		3.93E-15	5.76E-16	1.39E-15	2.35E-17	5.40E-15	1.18E-15	1.89E-15	2.95E-16
Max interference (dBm)		-114.05	-122.39	-118.57	-136.30	-112.68	-119.28	-117.23	-125.30
100 BPS ORIGINAL SYSTEM									
Turnaround C/No dB-Hz (dB)		46.53	38.65	43.54	35.64	48.71	40.84	45.72	37.84
Modulation Loss (dB)		1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20
Avaliable Eb/No (dB)		25.33	17.45	22.34	14.44	27.51	19.64	24.52	16.64
Required Eb/No (w/ 2 dB imp loss) (dB)		12.50	12.50	12.50	12.50	12.50	12.50	12.50	12.50
Margin (dB)		12.83	4.95	9.84	1.94	15.01	7.14	12.02	4.14

The link budget above reflects the modified budget showing the 306 BPS link. We are focused on the entry found under 1 link per satellite and using the weaker link which is the GOES I/M series, we see that the excess margin is

0.4 dB. It must be noted that this is on top of an additional 3 dB margin that has been included along with another 1.5 dB for modulation spreading loss.

APPENDIX F: PN Code Sequences for spread spectrum modulation

Table 2: Explicit PN Code Sequences (Binary)

Code	Sequence
GOES-E I	101101100010010010001001110001111000010100001110011001011111001101101110011010011110011110101010101110000001101101100010001001
GOES-E Q	000001111110101000110001100010111001000001100111010011000001011100000100011101100011101000010111101011100100010001110001001000
GOES-W I	100001100111000100101101011000000010100101001100001101010000101100110100011000010011011111010100111010110010101000101001101000
GOES-W Q	011001110100000101111000110001001011001100110111101100101111101011101100110001001100001010010110001101010101100010011010101001 0
Spare I	00101000011000100010100000111010010111101101111100000000000000100110110101011111110111100111110110110001100110011100 11000011011
Spare Q	00111011011001110110010011100000010011111000101100001111111010100000010000110100100100110111001101111010100000100101 0110110101

Table 3: Explicit PN Code Sequences (Hex)

Code	Sequence
GOES-E I	B6 24 89 C7 85 0E 65 F3 6E 69 E7 AA B8 1B 61 12
GOES-E Q	07 EA 31 8B 90 67 4C 17 04 76 3A 17 AE 44 71 20
GOES-W I	86 71 2D 60 14 A6 1A 85 9A 30 9B EA 75 95 14 D0
GOES-W Q	67 41 78 C4 B3 37 B2 FA EC C4 C2 96 35 58 9A A4
Spare I	28 62 28 3A 5E DF 00 02 6D 5F DE 7D B1 99 CC 36
Spare Q	3B 67 72 70 27 C5 87 F5 02 1A 49 B9 BD 41 2B 6A

APPENDIX G: *Suggested Authentication Implementation*

The following diagram illustrates the process of generating the authentication word, and of verifying it at the receiver:
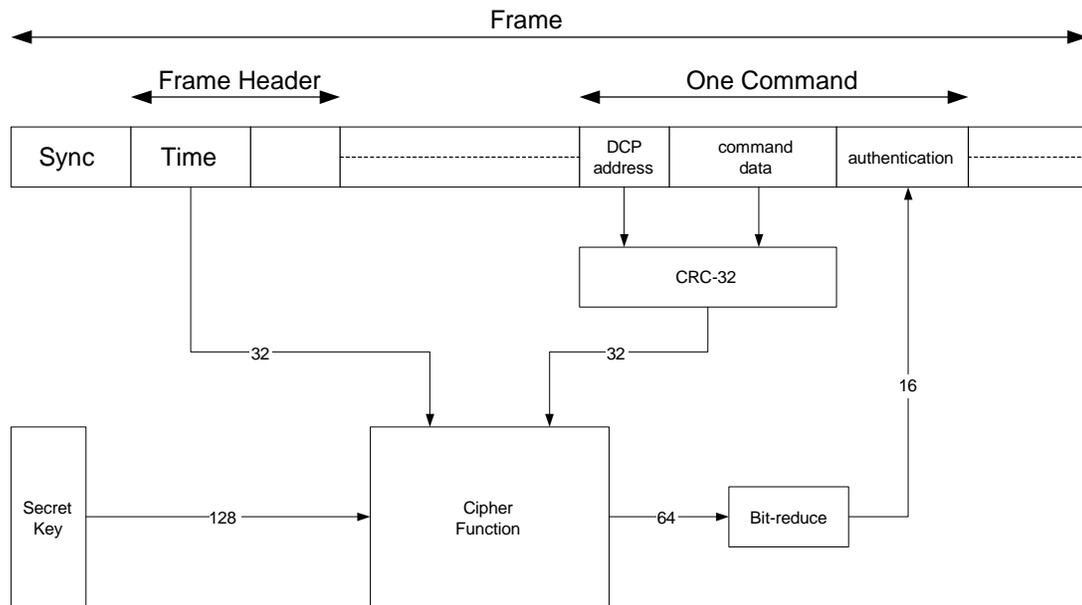
APPENDIX H: COMMANDS

The list provided here is just a sampling of the commands possible. Sutron will provide a 'COMMAND SET' list outside of this report that will provide greater details.

REMOTE FUNCTION COMMANDS:

The following list is a tentative list of potential commands that may be used to instruct, change or modify the behavior of a remote DCP.

> add group – adds an id to the group list
> remove group – removes an id from the group list
> clear all groups – removes an id from all group lists
> reset DCP – power off and on again
> reset failsafe --
> set DCP schedule – time, interval, channel, baud, duration
> set TX power – up/down or absolute
> receive file – named file transfer
> ack random – this can interact with adaptive random to reduce random transmissions.
> control – turn things on/off
> mode – set mode specific to the DCP
> measure – make the requested measurement
> transmit current data
> transmit old data
> transmit BIT or diagnostics
> transmit status
> transmit setup
> transmit tx format metadata
> set receiver dutycycle – allows remote setting of when the receiver is on and off to help conserve power.
> passthru – send data to the DCP.

Predefined commands:

This is a beginning of a list that may greatly expand as the needs are recognized and deemed valuable. These represent the core most common commands that may be used.

- "00"H   Filler
- "01"H   Reset
- "02"H   Chg TX info   2 bits baud, 10 bits chan, 18 bits time, 18 bits interval
- "03"H   Change TX power   2 bits (up, down, absolute), amount ?? bits (steps of 0.5dB)
- "FF"H   Passthru command
- "FE"H   File transfer
  Comment: Clarification will be necessary to transfer large blocks and split blocks across messages.

Command Acknowledgement:

Sutron proposes that each and every command will create a low priority acknowledgement. This will be done by setting a flag bit in the transmitter. The next scheduled transmission will relay the fact that the command was received and processed. This requires ZERO reply channel bandwidth which is potentially a bottleneck when commanding a large group of transmitters.

If a command to a platform requires a higher level of acknowledgement, then a transmit reply message may be sent. This will provide an efficient method of conserving transmit bandwidth.

Latency Issue for Addressing Many Platforms

The proposed DCP Command link is very efficient at addressing multiple platforms using the concept of Block IDs. Using the block IDs, many thousands of DCPs could be commanded with the same time making large scale commanding of all DCPs very possible from NESDIS's viewpoint in some case of an emergency.

The only scenario for a bottleneck would be the individual addressing of many thousands of platforms individually without the use of block commands. In this situation, the list of platforms to be addressed would stack up at NESDIS until they are able to send out at approx 6 commands per second rate. In this situation, it would be possible for a delay or latency in getting the command to the DCP.

APPENDIX I: Conservation Using Duty Cycle

One of the critical aspects of the DCP Command receiver is that it must operate on a very small power budget as the majority of users have these stations located in very remote locations that are not accessible to AC power. Therefore it is imperative that the system keep the power as low as possible so as not to exhaust the power budget afforded by a solar panel supplied battery. However, there may be a class of users with ample power available and would trade access time or other capabilities for power.

This leads to the general classification of sites based on power availability. These are simply:
Low Power Station (LP station)
High Response Station (HR station)
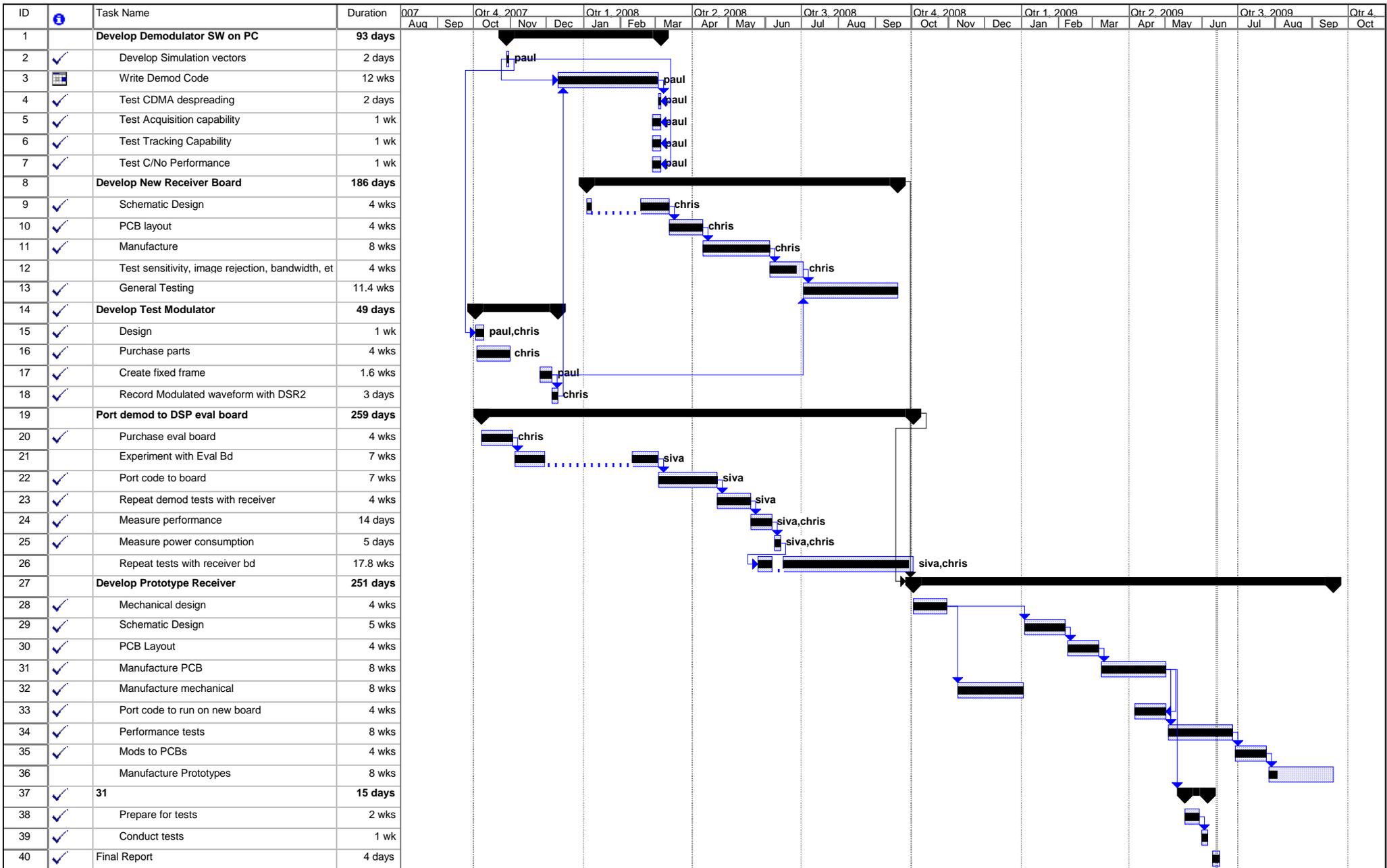
1. Low Power Station

The first or 'Low Power' station does not require the capability to respond to a command quickly and places a greater priority on the need for the lowest power consumption. This type of station must be of the nature that it will be acceptable to get a response from that station on the order of up to about 10 to 15 minutes worst case. This delay will be based on the concept that the station will have the DCP Command receiver turned off saving power. The powering of the receiver will be done on a schedule thereby creating periods in which the station will not be able to receive any commands from NESDIS.

2. High Response Station

The High Response capability station is a station that either has a need for very quick response to commands (some form of emergency situation monitoring) that may occur at any time or situations in which multiple commands may need to be sent in rapid succession falling out of the normal 'on time' window. Either of these would require very high duty cycles thereby increasing the power consumption. The NESDIS computer system shall be designed to know the settings of the remote station either by filling out tables, or by direct polling of the remote station with automatic generation of PDT type of information.

3. Compromise station.

The most likely operating scenario for the majority of stations would likely be the 'Low Power' type station. However, commands may be used to turn on the receiver for a period of time defined in an argument of the command. So, for example, a typical station may be in the low power mode as rarely is there a need to communicate to it. Say that a hurricane, major storm, or some other event is about to take place, the station may have its receiver forced on for a continuous period of time, from 10 minutes to days if necessary. This would allow virtual instantaneous response in emergency data taking conditions, but when the defined time interval passes, the station would revert to the low power mode thereby saving the battery power.

ID		Task Name	Duration
1		**Develop Demodulator SW on PC**	**93 days**
2	✓	Develop Simulation vectors	2 days
3	📋	Write Demod Code	12 wks
4	✓	Test CDMA despreading	2 days
5	✓	Test Acquisition capability	1 wk
6	✓	Test Tracking Capability	1 wk
7	✓	Test C/No Performance	1 wk
8		**Develop New Receiver Board**	**186 days**
9	✓	Schematic Design	4 wks
10	✓	PCB layout	4 wks
11	✓	Manufacture	8 wks
12		Test sensitivity, image rejection, bandwidth, et	4 wks
13	✓	General Testing	11.4 wks
14	✓	**Develop Test Modulator**	**49 days**
15	✓	Design	1 wk
16	✓	Purchase parts	4 wks
17	✓	Create fixed frame	1.6 wks
18	✓	Record Modulated waveform with DSR2	3 days
19		**Port demod to DSP eval board**	**259 days**
20	✓	Purchase eval board	4 wks
21		Experiment with Eval Bd	7 wks
22	✓	Port code to board	7 wks
23	✓	Repeat demod tests with receiver	4 wks
24	✓	Measure performance	14 days
25	✓	Measure power consumption	5 days
26		Repeat tests with receiver bd	17.8 wks
27		**Develop Prototype Receiver**	**251 days**
28	✓	Mechanical design	4 wks
29	✓	Schematic Design	5 wks
30	✓	PCB Layout	4 wks
31	✓	Manufacture PCB	8 wks
32	✓	Manufacture mechanical	8 wks
33	✓	Port code to run on new board	4 wks
34	✓	Performance tests	8 wks
35	✓	Mods to PCBs	4 wks
36		Manufacture Prototypes	8 wks
37	✓	**31**	**15 days**
38	✓	Prepare for tests	2 wks
39	✓	Conduct tests	1 wk
40	✓	Final Report	4 days

Project: DCP Command Receiver Jun
Date: Sat 06/13/09

Task		Progress		Summary		External Tasks		Deadline
Split	⋯⋯⋯	Milestone	◆	Project Summary		External Milestone	◆	

Page 1